



Description

The XPX80N023LL uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

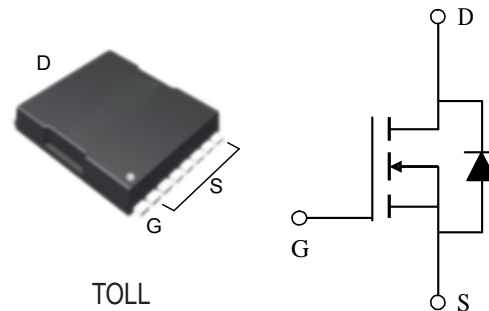
Application

- PWM
- Load Switching

$V_{DS} = 80V, I_D = 200A$

$R_{DS(ON)} = 2.1m\Omega$ (typ) @ $V_{GS} = 10V$

$R_{DS(ON)} = 2.6m\Omega$ (typ) @ $V_{GS} = 4.5V$



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
XPX80N023LL	XPX80N023LL	TOLL	-	-	2000

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	200	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	120	A
Pulsed Drain Current	I_{DM}	610	A
Maximum Power Dissipation	P_D	231	W
Derating factor		1.85	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	552	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$
Thermal Resistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	0.68	$^\circ C/W$

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

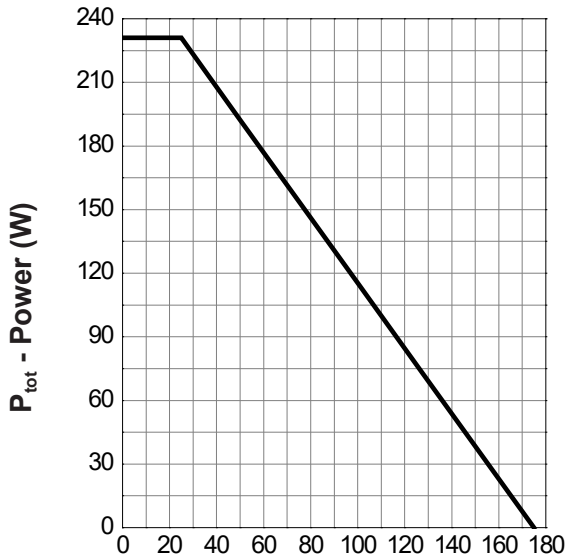
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	80	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=64V, V_{GS}=0V$	-	-	1	μA
		$T_J=85^\circ C$	-	-	30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	2	3	4	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
$R_{DS(ON)}^c$	Drain-Source On-state Resistance	$V_{GS}=10V, I_{DS}=80A$	-	2.1	2.9	$m\Omega$
Diode Characteristics						
V_{SD}^c	Diode Forward Voltage	$I_{SD}=40A, V_{GS}=0V$	-	0.8	1.1	V
t_{rr}^d	Reverse Recovery Time	$I_{SD}=80A, di_{SD}/dt=100A/\mu s$	-	65	-	ns
Q_{rr}^d	Reverse Recovery Charge		-	113	-	nC
Dynamic Characteristics^d						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1MHz$	-	1	-	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=50V,$ Frequency=1.0MHz	-	5500	7150	pF
C_{oss}	Output Capacitance		-	873	-	
C_{riss}	Reverse Transfer Capacitance		-	117	-	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=30V, R_L=30\Omega,$ $I_{DS}=1A, V_{GEN}=10V,$ $R_G=6\Omega$	-	34	61	ns
t_r	Turn-on Rise Time		-	15	28	
$t_{d(OFF)}$	Turn-off Delay Time		-	81	145	
t_f	Turn-off Fall Time		-	156	280	
Gate Charge Characteristics^d						
Q_g	Total Gate Charge	$V_{DS}=50V, V_{GS}=10V,$ $I_{DS}=80A$	-	82	115	nC
Q_{gs}	Gate-Source Charge		-	30	-	
Q_{gd}	Gate-Drain Charge		-	16	-	

Note c : Pulse test ; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

Note d : Guaranteed by design, not subject to production testing.

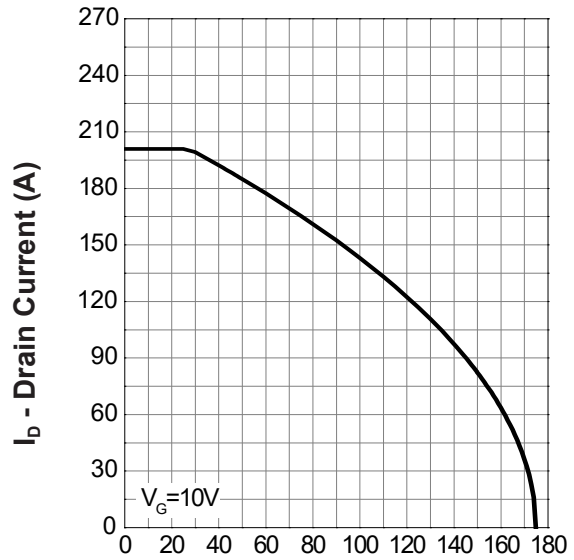
Typical Operating Characteristics

Power Dissipation



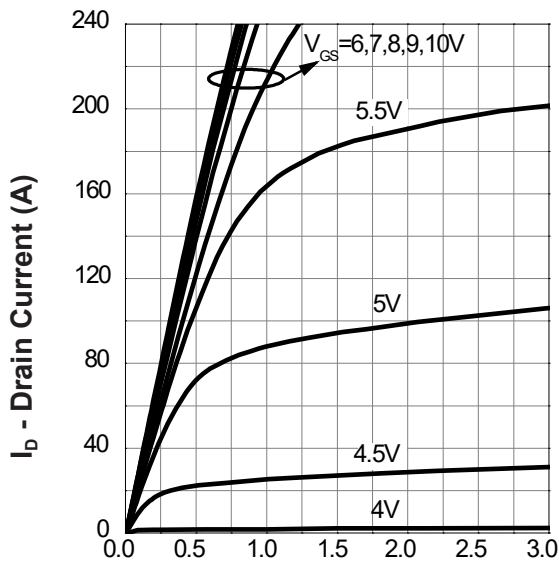
T_c - Case Temperature (°C)

Drain Current



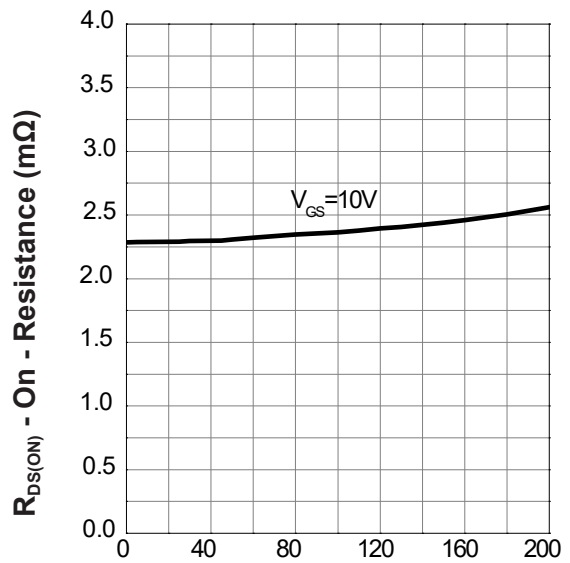
T_c - Case Temperature (°C)

Output Characteristics



V_{DS} - Drain - Source Voltage (V)

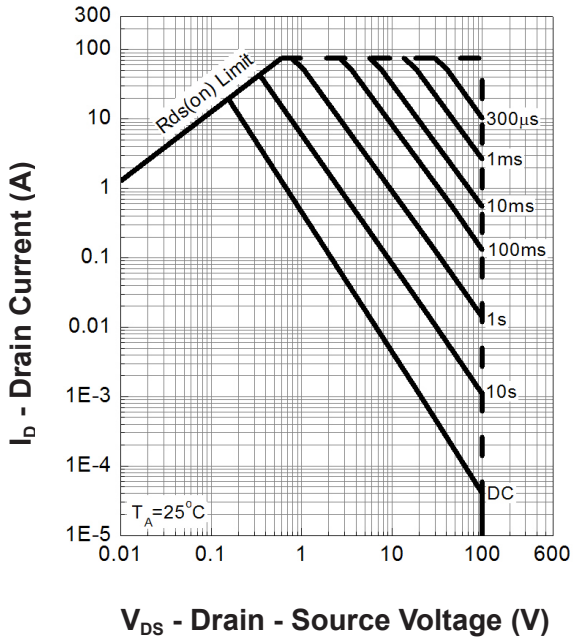
Drain-Source On Resistance



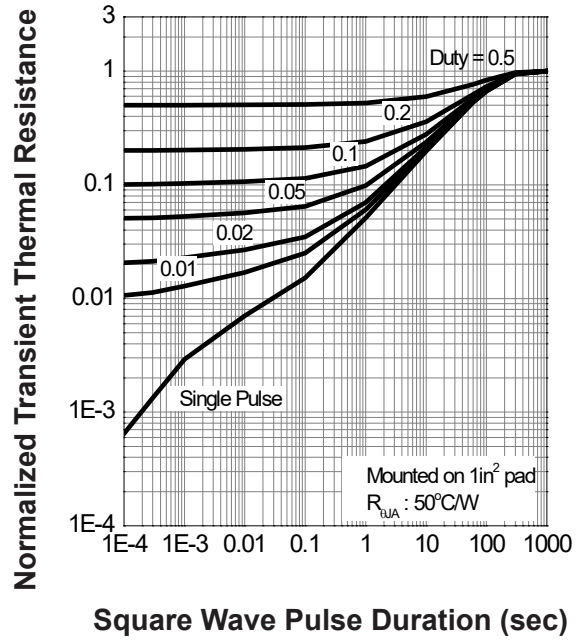
I_D - Drain Current (A)

Typical Operating Characteristics(Cont.)

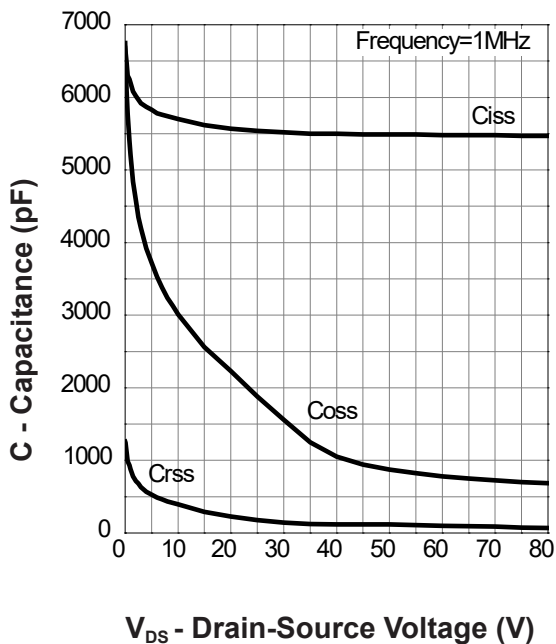
Safe Operation Area



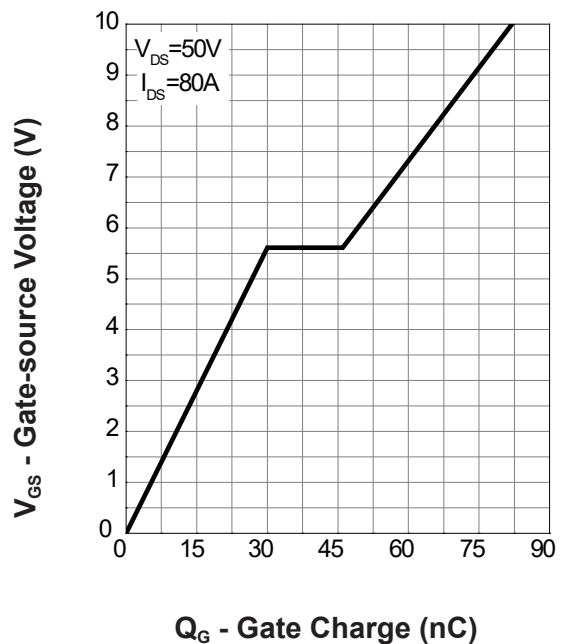
Thermal Transient Impedance



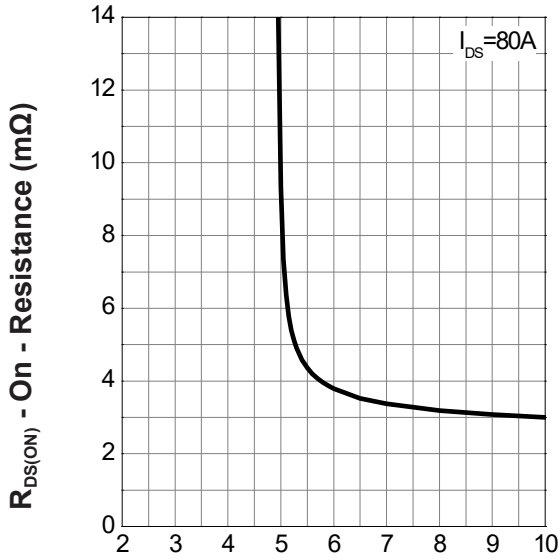
Capacitance



Gate Charge

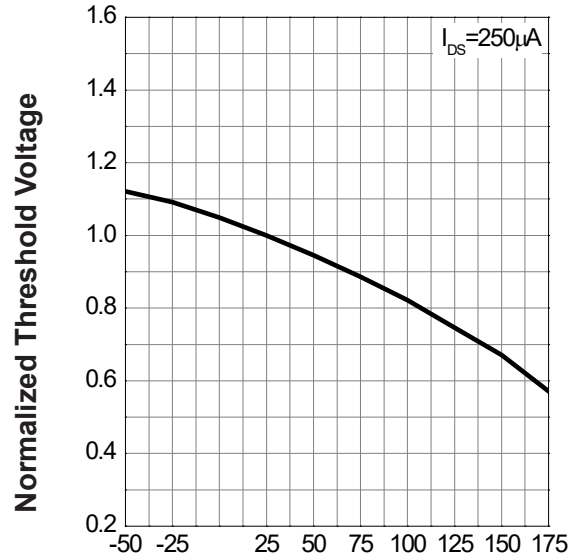


Gate-Source On Resistance



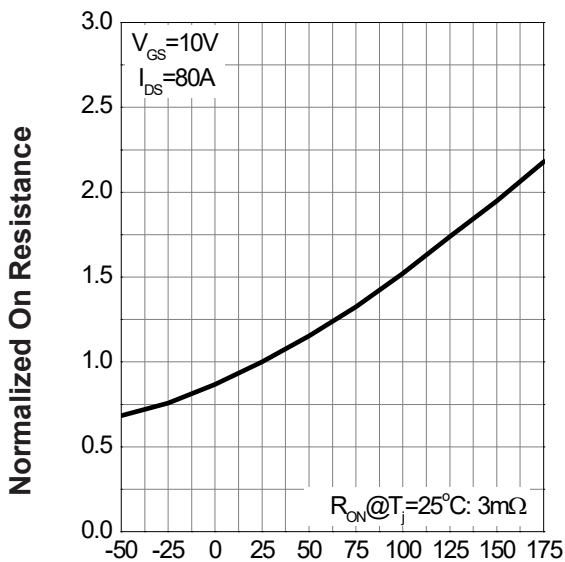
V_{GS} - Gate - Source Voltage (V)

Gate Threshold Voltage



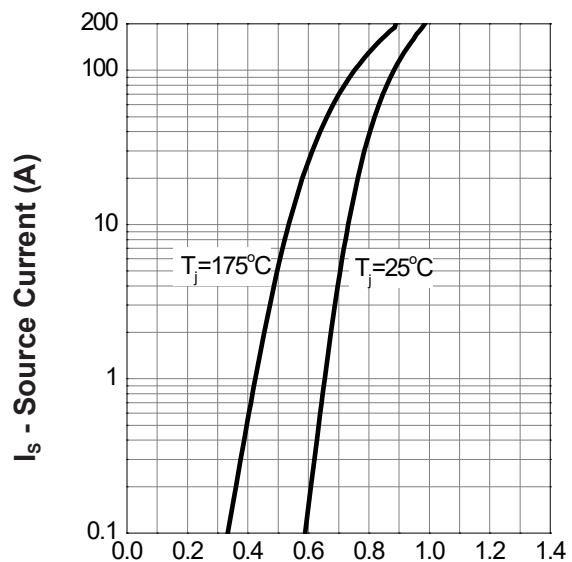
T_J - Junction Temperature (°C)

Drain-Source On Resistance



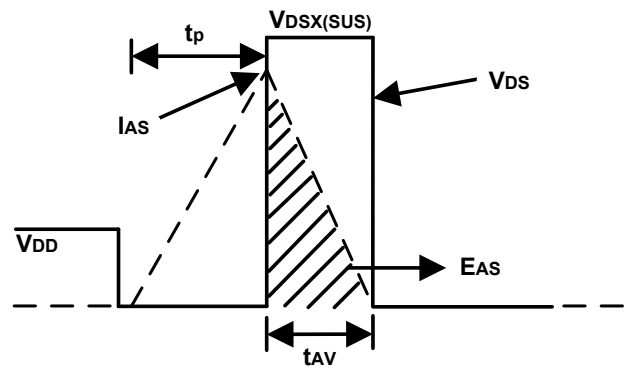
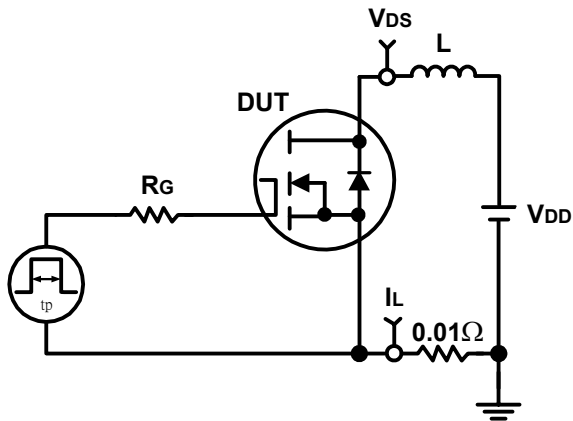
T_J - Junction Temperature (°C)

Source-Drain Diode Forward

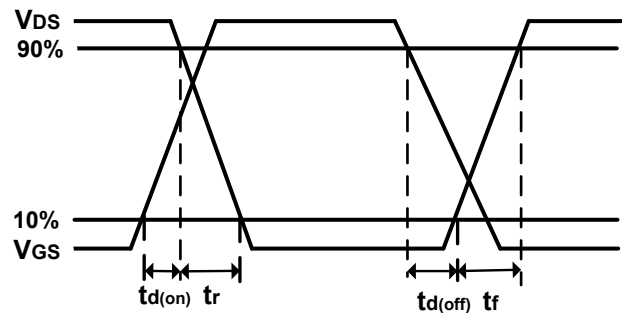
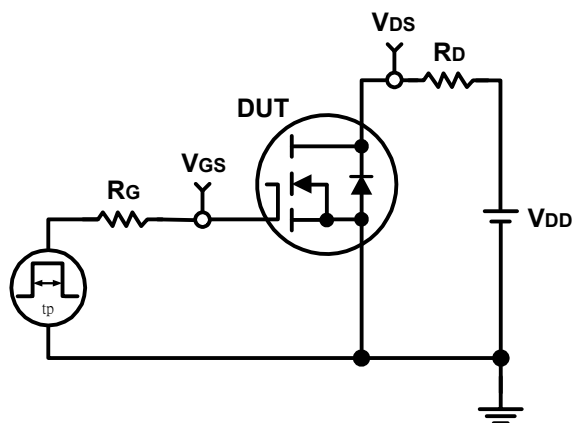


V_{SD} - Source - Drain Voltage (V)

Avalanche Test Circuit and Waveforms

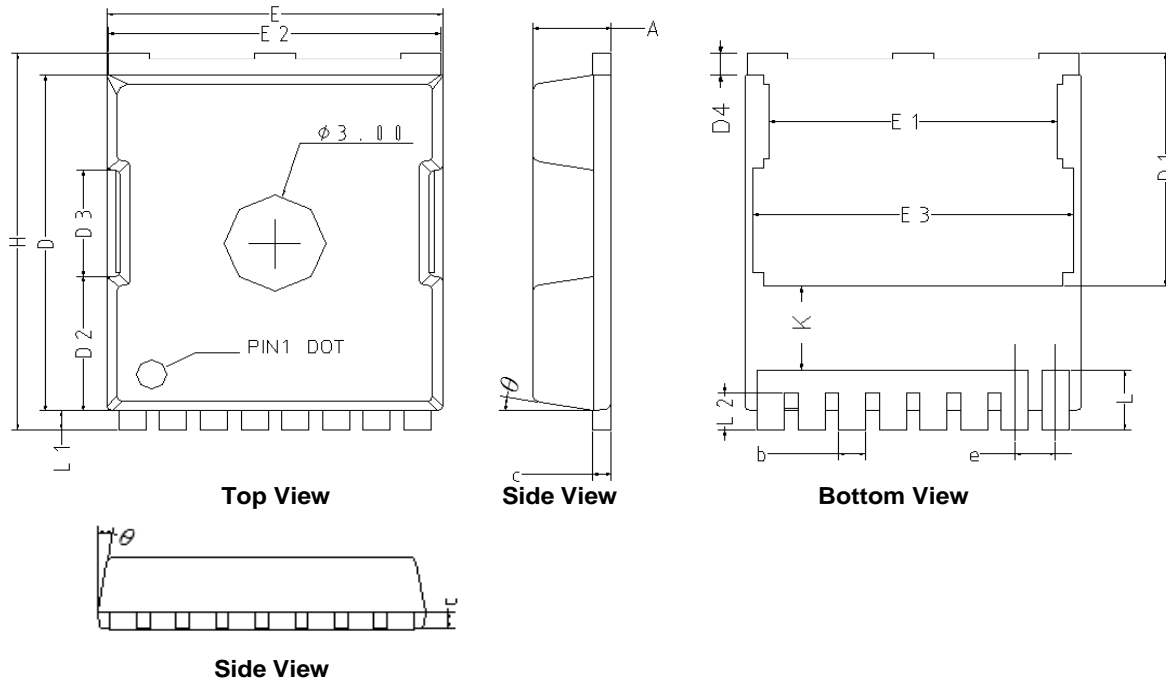


Switching Time Test Circuit and Waveforms



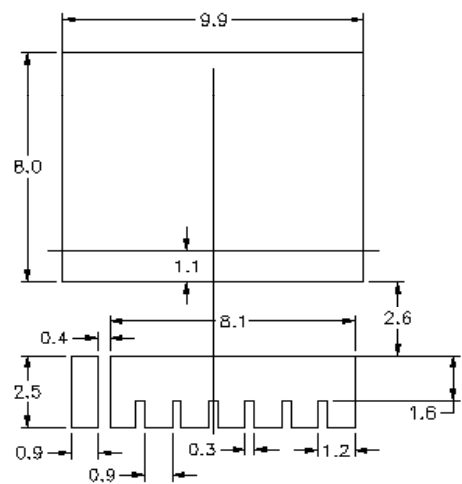
Package Information

TOLL



SYMBOLS	TO-LL			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.20	2.40	0.087	0.094
b	0.70	0.90	0.028	0.035
c	0.40	0.60	0.016	0.024
D	10.23	10.63	0.403	0.419
D1	7.05	7.45	0.278	0.293
D2	3.98	4.38	0.157	0.172
D3	3.10	3.50	0.122	0.138
D4	0.50	0.90	0.020	0.035
E	9.70	10.10	0.382	0.398
E1	8.30	8.70	0.327	0.343
E2	9.60	10.00	0.378	0.394
E3	9.26	9.66	0.365	0.380
H	11.53	11.93	0.454	0.470
e	1.2 BSC		0.0472 BSC	
K	2.43	2.83	0.096	0.111
L	1.65	2.05	0.065	0.081
L1	0.40	0.80	0.016	0.031
L2	0.95	1.35	0.037	0.053
θ	6°	10°	6°	10°

RECOMMENDED LAND PATTERN



UNIT: mm

80V N-Channel Enhancement Mode MOSFET

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245°C ±5°C	5sec ±1 sec
Pb-Free device	260°C +0/-5°C	5sec ±1 sec



This integrated circuit can be damaged by ESD. UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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