30V N+P-Channel Enhancement Mode MOSFET

RoHS COMPLIANT

Description

The XPX4616XS uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge . The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

V_{DS} =30V,I_D =12A

$R_{DS(ON)}$=11mΩ (typ) @ V_{GS}=10V

$R_{DS(ON)}$=15mΩ (typ) @ V_{GS}=4.5V

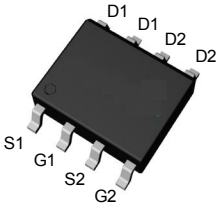
V_{DS} =-30V,I_D =-12A

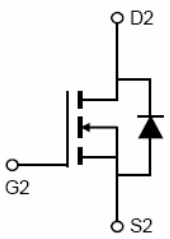
$R_{DS(ON)}$=16mΩ (typ) @ V_{GS}=10V

$R_{DS(ON)}$=19mΩ (typ) @ V_{GS}=4.5V

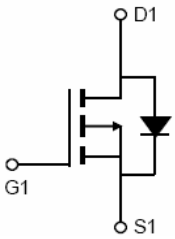
General Features

- High power and current handing capability
- Lead free product is acquired
- Surface mount package





N-channel



P-channel

Product ID	Pack	Marking	Qty(PCS)
XPX4616XS	SOP-8	XPX4616XS XXX YYYY	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
VDS	Drain-Source Voltage	30	-30	V
VGS	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	12	-12	A
I_D@T_A=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	10	-8	A
IDM	Pulsed Drain Current[2]	52	-45	A
EAS	Single Pulse Avalanche Energy[3]	22	45	mJ
IAS	Avalanche Current	21	-30	A
P_D@T_A=25℃	Total Power Dissipation[4]	18	18	W
TSTG	Storage Temperature Range	-55 to 150	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	℃
RθJA	Thermal Resistance Junction-Ambient [1]	55		℃/W
RθJA	Thermal Resistance Junction-Ambient[1],(t<=10sec)	5		℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	30	32.5	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=10A	---	11	16	mΩ
		V_{GS}=4.5V , I_D=8A	---	15	20	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.0	1.6	2.5	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=24V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=10A	---	16	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	2.5	5	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=20V , V_{GS}=4.5V , I_D=10A	---	7.2	---	nC
Q_{gs}	Gate-Source Charge		---	1.4	---	
Q_{gd}	Gate-Drain Charge		---	2.2	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=15V , V_{GS}=10V , R_G=3.3Ω, I_D=5A	---	4.1	---	ns
T_r	Rise Time		---	9.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	15.5	---	
T_f	Fall Time		---	6.0	---	
C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	816	---	pF
C_{oss}	Output Capacitance		---	81	---	
C_{rss}	Reverse Transfer Capacitance		---	65	---	
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	12	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1.2	V

Note :

1、The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=12A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Electrical Characteristics (T_C=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-30	-33	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-7A	---	16	19	mΩ
		V_{GS}=-4.5V , I_D=-5A	---	19	30	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.0	---	-2.5	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-24V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=-24V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-7A	---	15	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz		15	30	
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-20V , V_{GS}=-4.5V , I_D=-7A	---	9.8	---	nC
Q_{gs}	Gate-Source Charge		---	2.2	---	
Q_{gd}	Gate-Drain Charge		---	3.4	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V , V_{GS}=-10V , R_G=3.3 , I_D=-5A	---	16.4	---	ns
T_r	Rise Time		---	20.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	55	---	
T_f	Fall Time		---	10	---	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	985	---	pF
C_{oss}	Output Capacitance		---	148	---	
C_{rss}	Reverse Transfer Capacitance		---	115	---	
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	-12	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1.2	V

Note :

1、The data tested by surface mo unted on a 1 inch^2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is V^{DD}=-25V,VGS=-10V,L=0.1mH,I^{AS}=-12A

4、The power dissipation is limited by 150℃ junction temperature

5 、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Typical Characteristics

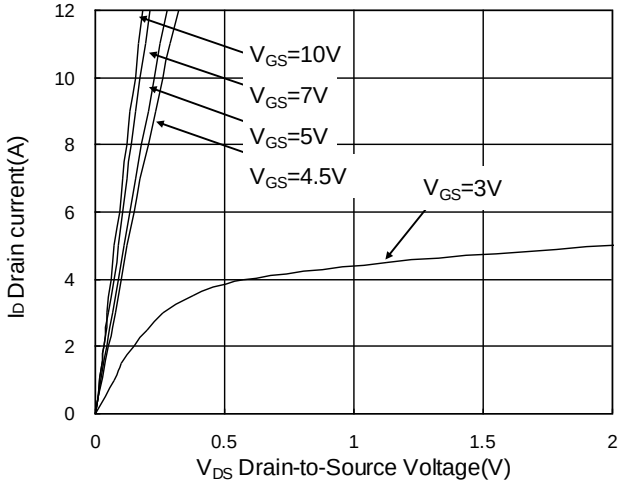


Fig.1 Typical Output Characteristics

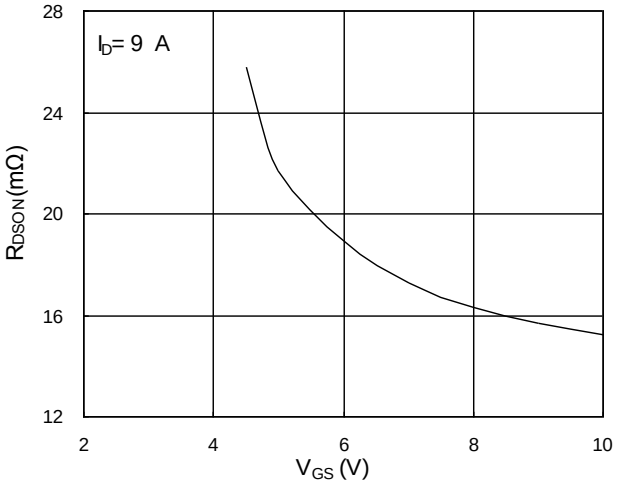


Fig.2 On-Resistance v.s Gate-Source

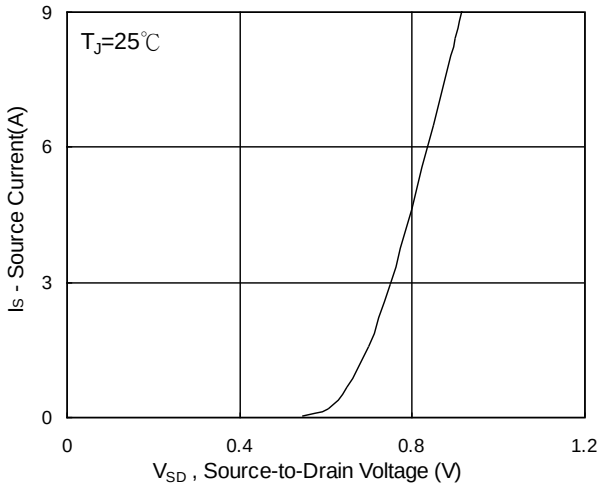


Fig.3 Forward Characteristics Of Reverse

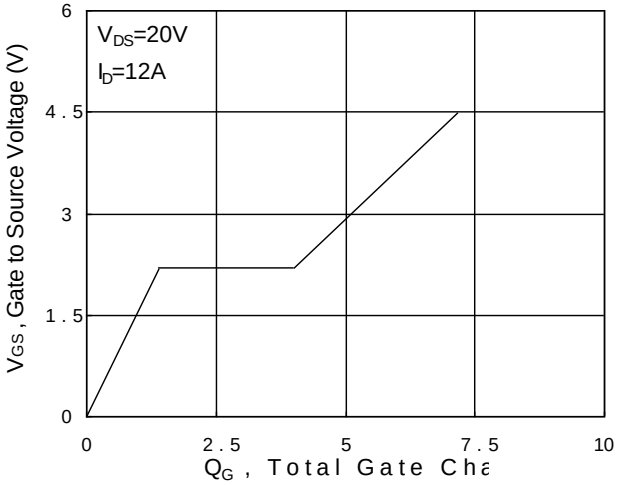


Fig.4 Gate-Charge characteristics

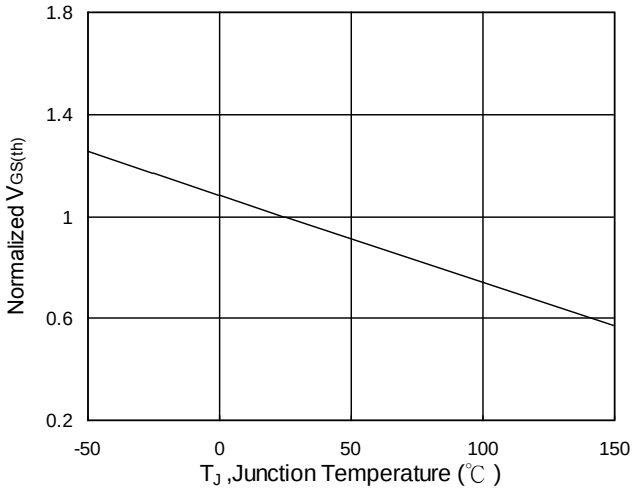


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

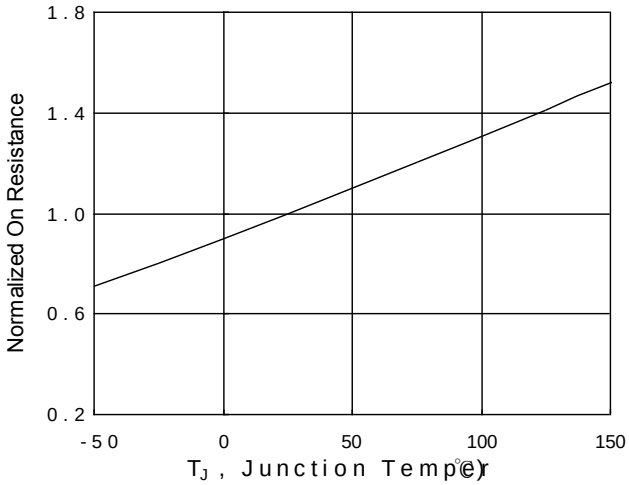


Fig.6 Normalized R_{DSON} v.s T_J

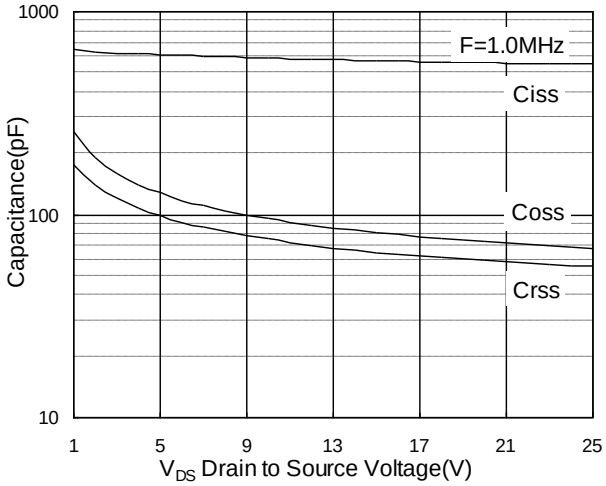


Fig.7 Capacitance

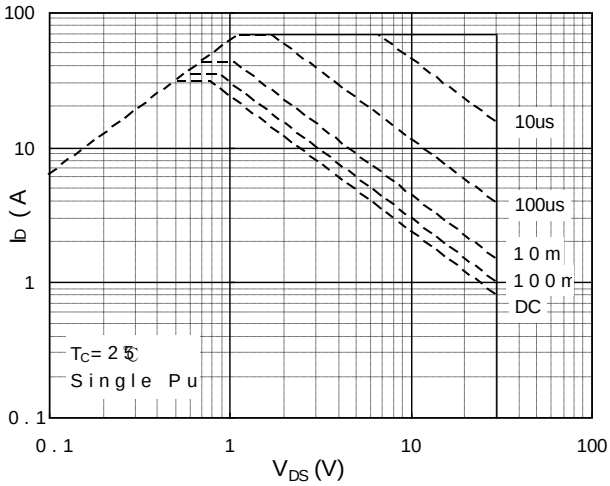


Fig.8 Safe Operating Area

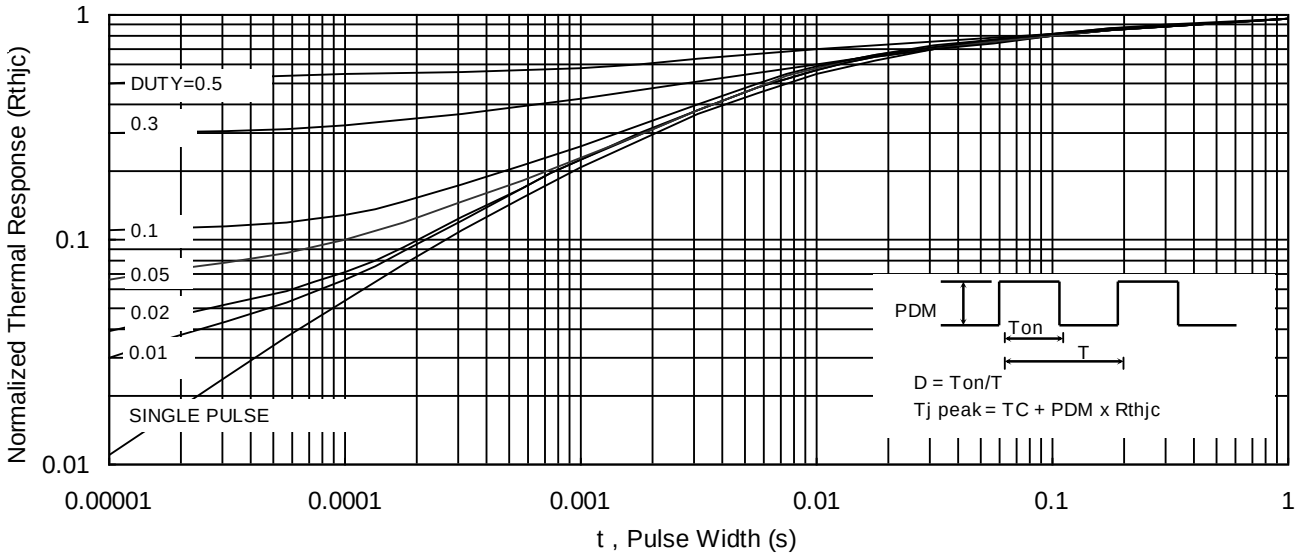


Fig.9 Normalized Maximum Transient Thermal Impedance

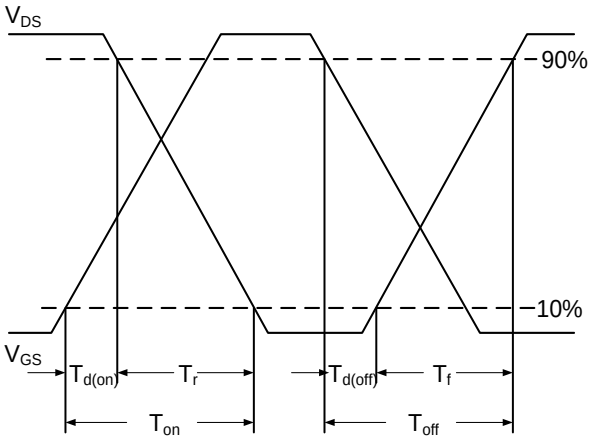


Fig.10 Switching Time Waveform

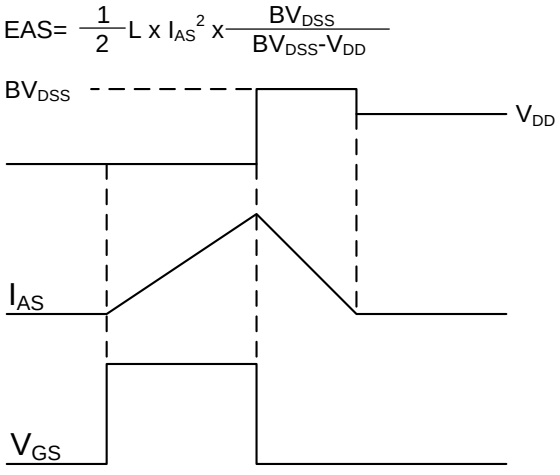


Fig.11 Unclamped Inductive Waveform

P-Typical Characteristics

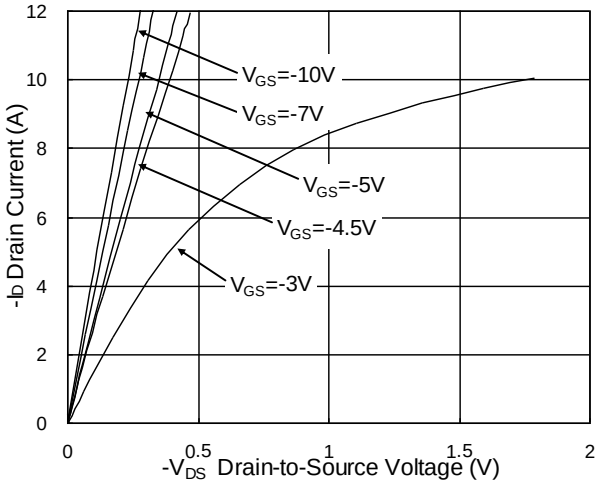


Fig.1 Typical Output Characteristics

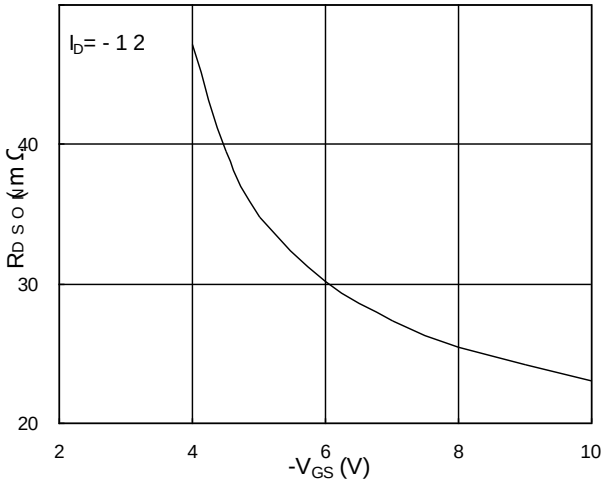
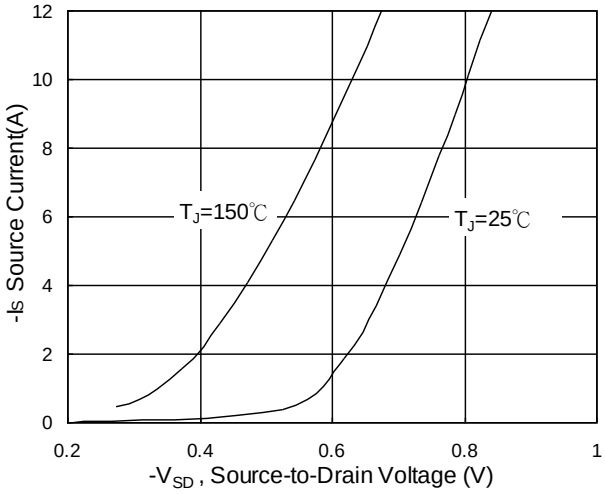


Fig.2 On-Resistance v.s Gate-Source



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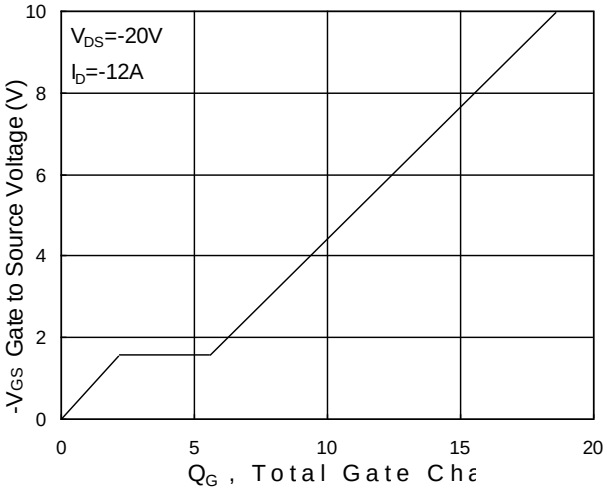


Fig.4 Gate-Charge Characteristics

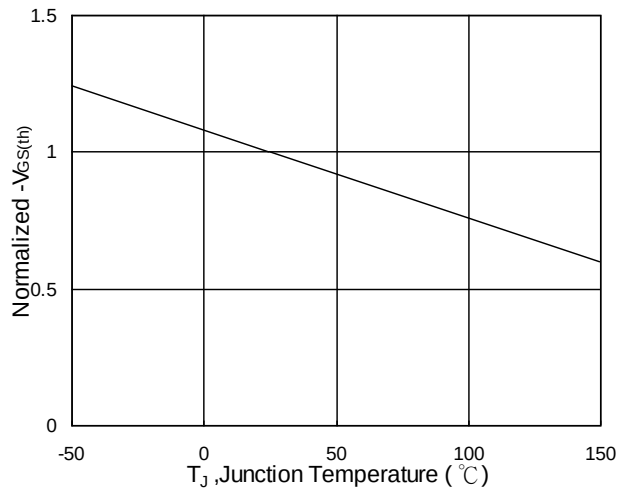


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

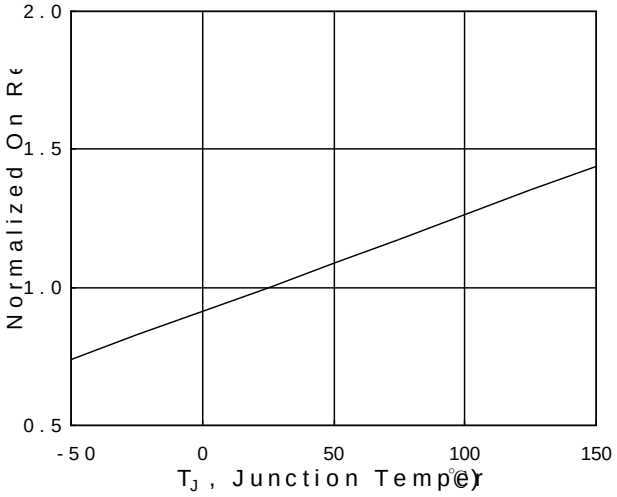


Fig.6 Normalized R_{DSON} v.s T_J

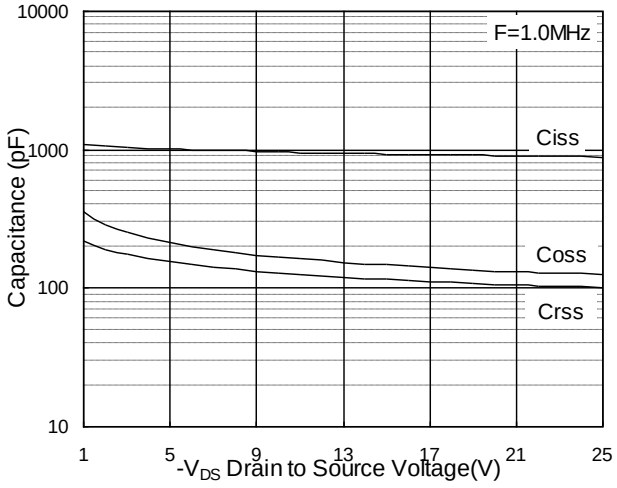


Fig.7 Capacitance

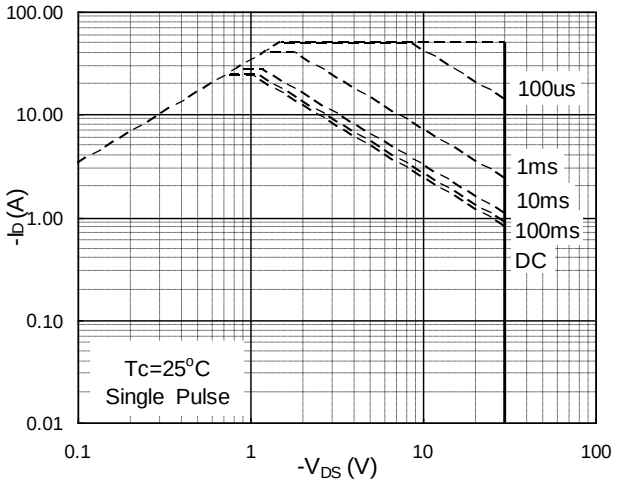
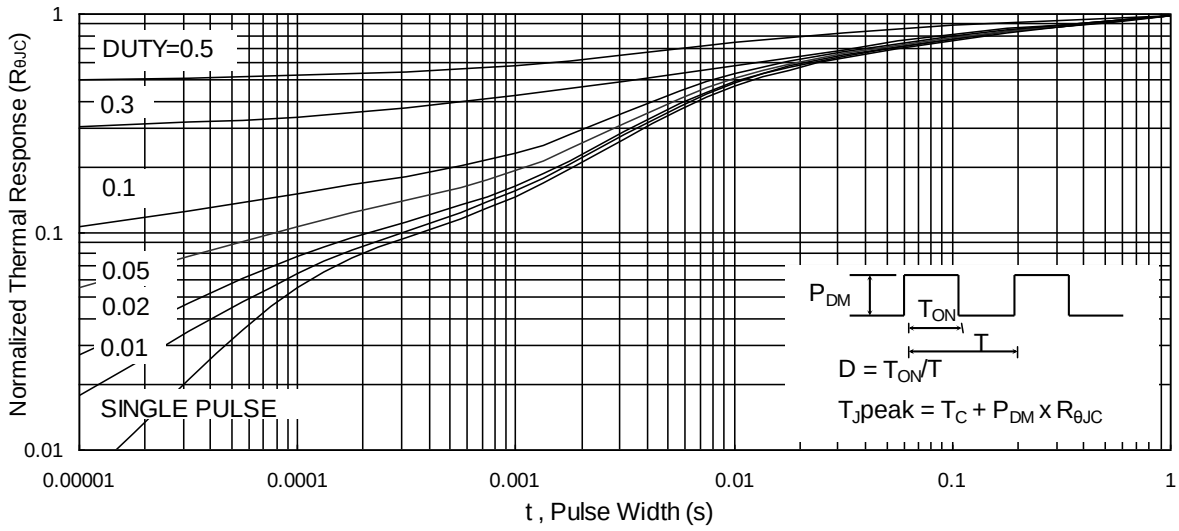


Fig.8 Safe Operating Area



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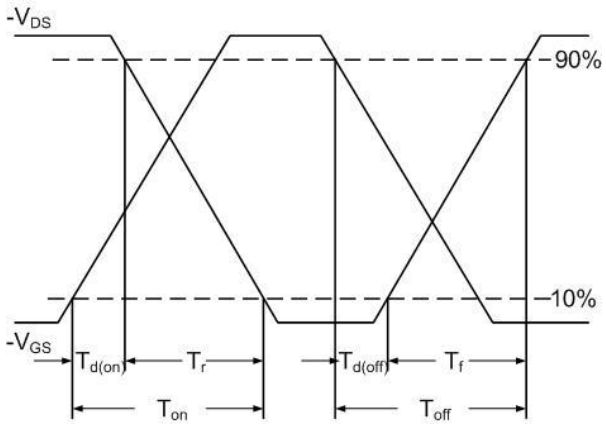


Fig.10 Switching Time Waveform

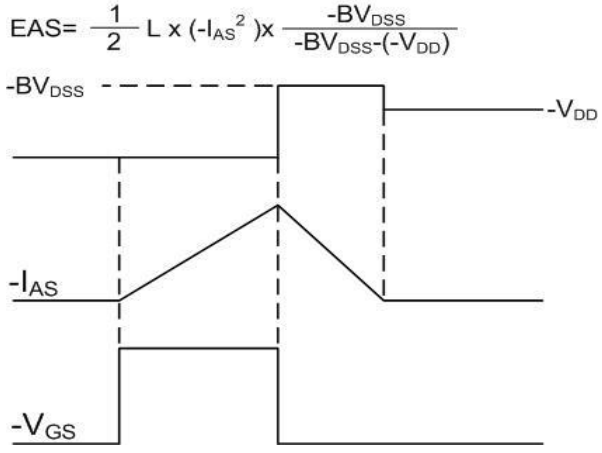
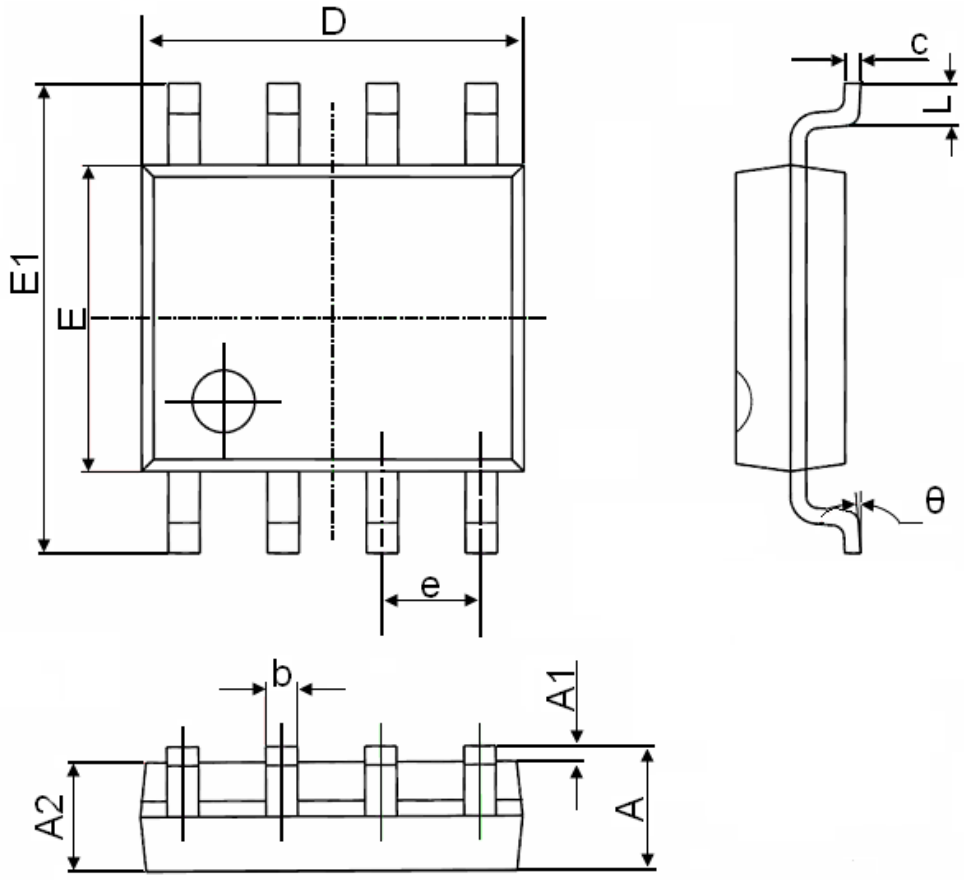


Fig.11 Unclamped Inductive Waveform

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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