-40V P-Channe Enhancement Mode MOSFET

RoHS COMPLIANT

Description

The XPX4025RX uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

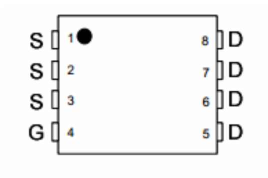
V_{DS} =-40V,I_D =-40A

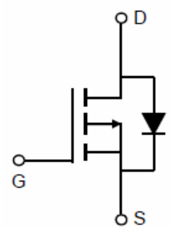
$R_{DS(ON)}$=13mΩ (typ) @ V_{GS}=-10V

$R_{DS(ON)}$=18mΩ (typ) @ V_{GS}=-4.5V

General Features

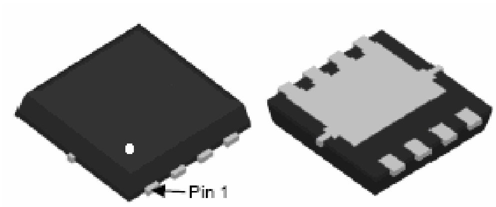
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation





Application

- Load switch
- Battery protection



DFN 3.3x3.3-8L

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
XPX4025RX	PDFN3*3-8L	XPX4025RX XXX YYYY	5000

Absolute Maximum Ratings (TC=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25˚C	Continuous Drain Current, V_{GS} @ -10V[1]	-40	A
I_D@T_C=100˚C	Continuous Drain Current, V_{GS} @ -10V[1]	-23	A
I_{DM}	Pulsed Drain Current[2]	-120	A
EAS	Single Pulse Avalanche Energy[3]	125	mJ
P_D@T_C=25˚C	Total Power Dissipation[4]	25	W
P_D@T_A=25˚C	Total Power Dissipation[4]	16	W
T_{STG}	Storage Temperature Range	-55 to 150	˚C
T_J	Operating Junction Temperature Range	-55 to 150	˚C
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	85	˚C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	5	˚C/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-40	-44	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.023	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-30A	---	13	18	mΩ
		V_{GS}=-4.5V , I_D=-20A	---	18	24	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D=-250uA	-1.0	-1.6	-2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.74	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-40V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=-40V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-20V , V_{GS}=-4.5V , I_D=-12A	---	25	---	nC
Q_{gs}	Gate-Source Charge		---	11	---	
Q_{gd}	Gate-Drain Charge		---	9.5	---	
$T_{d(on)}$	Turn-On Delay Time	VDD =-15V, RL=15Ω ID =-1A, VGEN =-10V, RG =6Ω	---	48	---	ns
T_r	Rise Time		---	24	---	
$T_{d(off)}$	Turn-Off Delay Time		---	88	---	
T_f	Fall Time		---	9.6	---	
C_{iss}	Input Capacitance	V_{DS}=-20V , V_{GS}=0V , f=1MHz	---	2188	---	pF
C_{oss}	Output Capacitance		---	260	---	
C_{rss}	Reverse Transfer Capacitance		---	85	---	
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	-40	A
I_{SM}	Pulsed Source Current[2,5]		---	---	-90	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1.3	V

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is VDD=-32V,VGS=-10V,L=0.1mH,IAS=-30A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

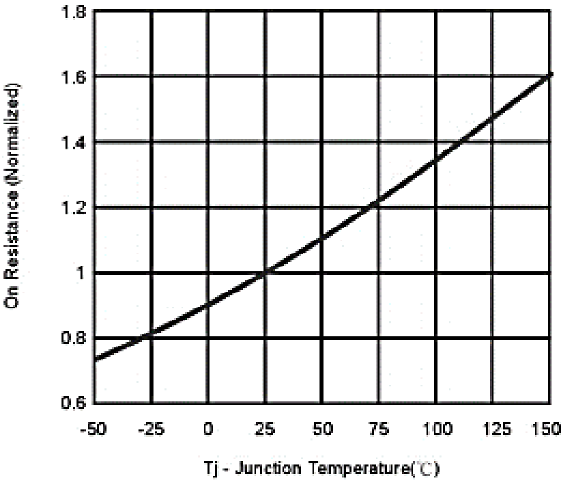


Fig.1 On Resistance Vs Junction Temperature

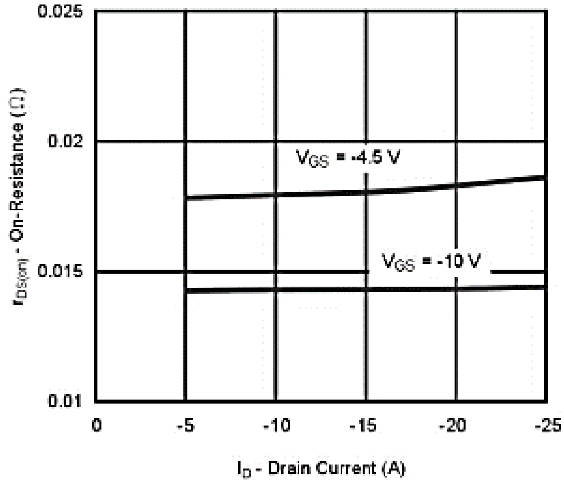


Fig.2 On-Resistance Vs.Drain Current

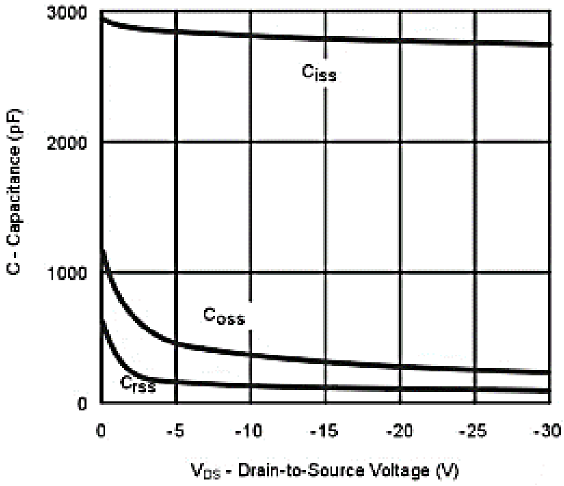


Fig.3 Capacitance

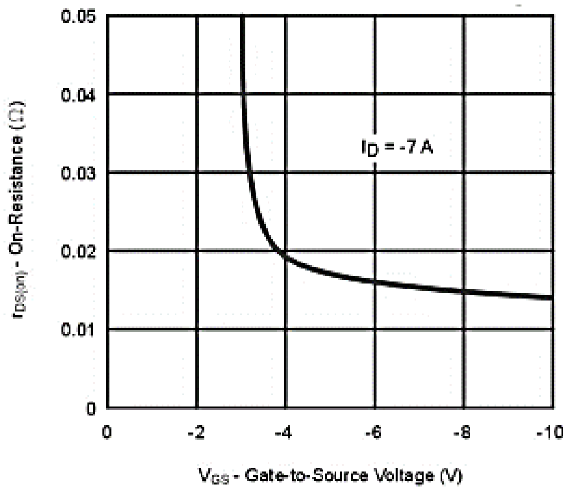


Fig.4 On-Resistance Vs. Gate-to-Sourece Voltage

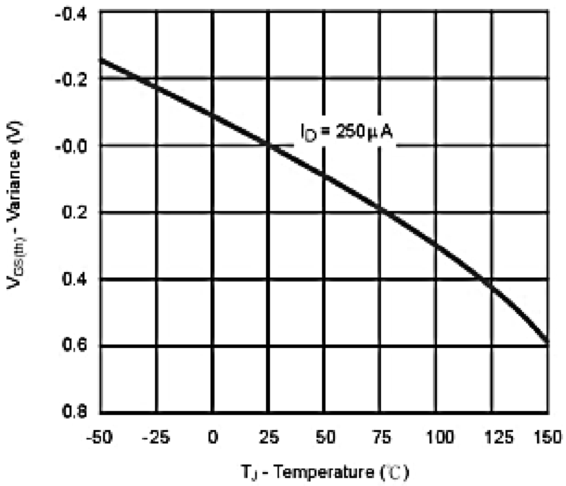


Fig.5 Threshold Voltage

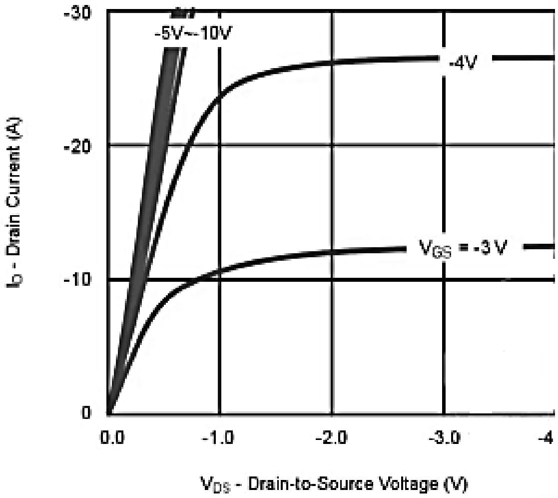


Fig.6 On-Region Characteristics

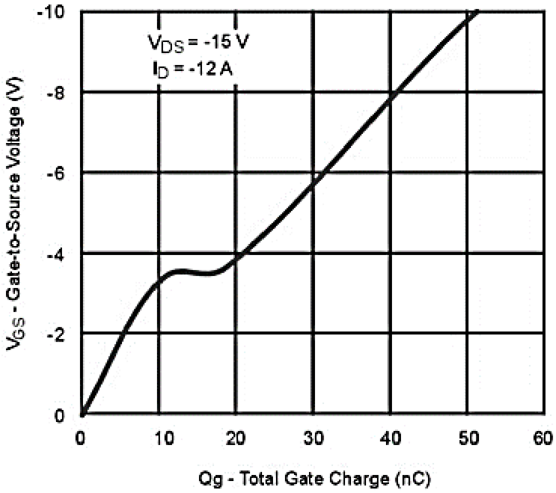


Fig.7 Gate Charge

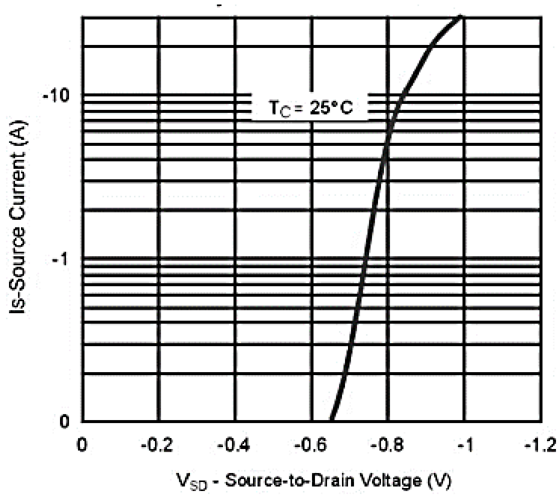


Fig.8 Body-diode Characteristice

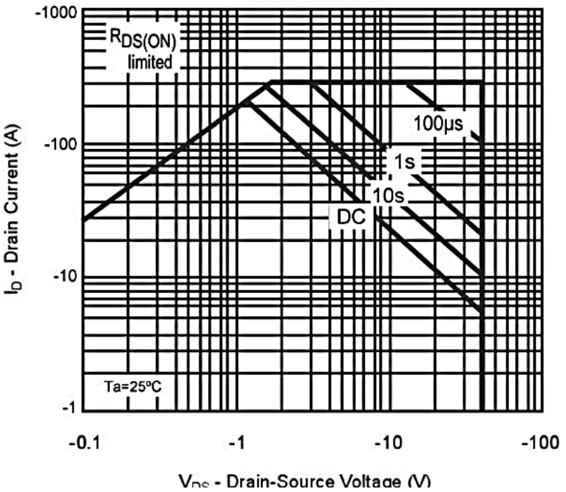


Fig.9 Safe Operating Area

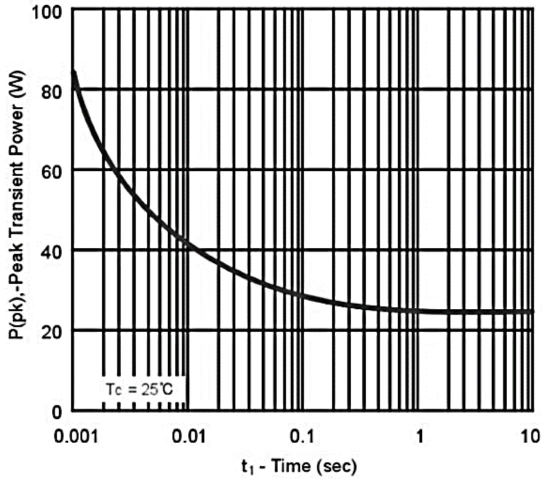


Fig.10 Single Pluse Maximum Power Dissipation

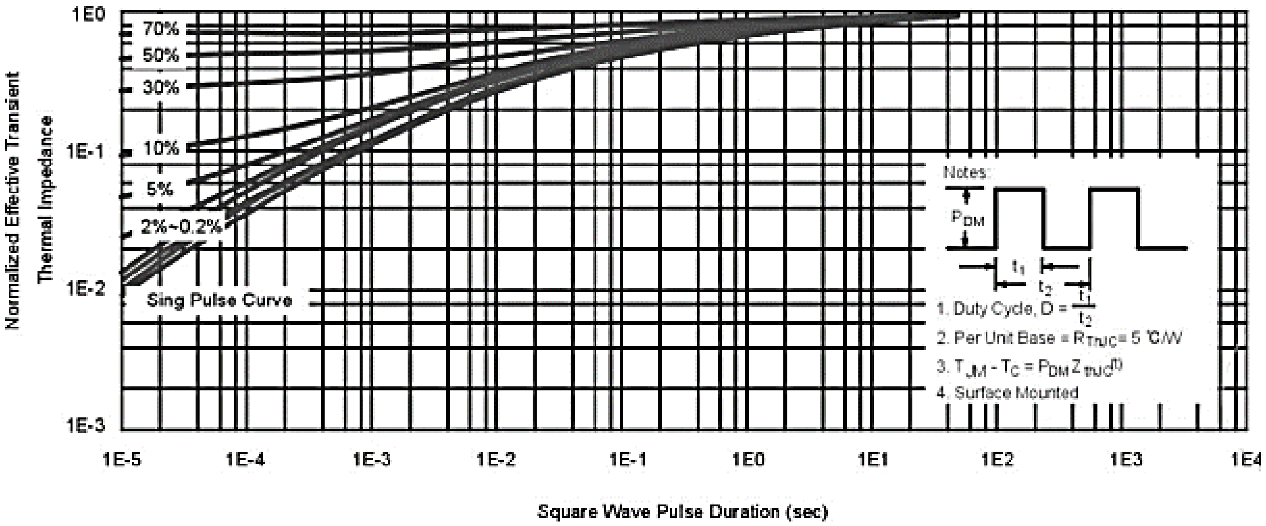
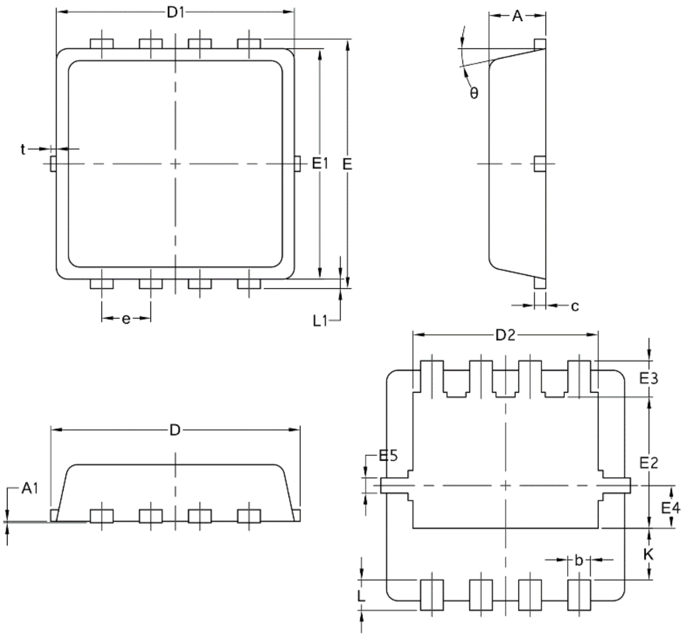


Fig.11 Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-DFN3*3-8L-JQ Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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