-20 P-Channel Enhancement Mode Power MOSFET

Description

The XPX2339AS uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications.

V_{DS} =-20V,I_D =-7.2A

$R_{DS(ON)}$=17mΩ (typ) @ V_{GS}=-4.5V

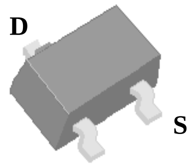
$R_{DS(ON)}$=20mΩ (typ) @ V_{GS}=-2.5V

General Features

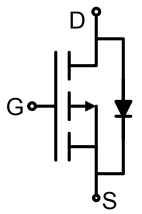
- High power and current handing capability
- Lead free product is acquired
- Surface mount package

Application

- PWM applications
- Load switch
- Power management



SOT23-3L



Schematic diagram

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
2339	XPX2339AS	SOT-23-3L	Ø180mm	8 mm	3000 units

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	-7.2	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-6.0	A
Drain Current-Pulsed (Note 1)	I_{DM}	-40	A
Maximum Power Dissipation	P_D	1.8	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃
Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	98	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-20	-22	---	V
△BVDSS/△TJ	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.01	---	V/℃
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=-4.5V , I_D=-4A	---	17	21	mΩ
		V_{GS}=-2.5V , I_D=-3A	---	20	28	
		V_{GS}=-1.8V , I_D=-1.5A		28	35	
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-0.4	-0.7	-1.0	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	2.96	---	mV/℃
IDSS	Drain-Source Leakage Current	V_{DS}=-16V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-16V , V_{GS}=0V , T_J=55℃	---	---	-5	
IGSS	Gate-Source Leakage Current	V_{GS}=±12V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-4A	---	21	---	S
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-15V , V_{GS}=-4.5V , I_D=-4A	---	27.3	38.2	nC
Q_{gs}	Gate-Source Charge		---	3.6	5.0	
Q_{gd}	Gate-Drain Charge		---	6.5	9.1	
Td(on)	Turn-On Delay Time	V_{DD}=-10V, V_{GS}=-4.5V , R_G=3.3Ω I_D=-4A	---	9.2	18.4	ns
T_r	Rise Time		---	59	106	
Td(off)	Turn-Off Delay Time		---	99	198	
T_f	Fall Time		---	71	142	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	2280	3192	pF
Coss	Output Capacitance		---	220	308	
Crss	Reverse Transfer Capacitance		---	187	262	
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	-4.7	A
I_{SM}	Pulsed Source Current[2,4]		---	---	-18.8	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1	V
t_{rr}	Reverse Recovery Time	I_F=-4A , dI/dt=100A/µs , T_J=25℃	---	52	---	nS
Q_{rr}	Reverse Recovery Charge		---	28	---	nC

Note :

1.The data tested by surface mounted on a 1 inch[2] FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
3.The power dissipation is limited by 150℃ junction temperature
4 .The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

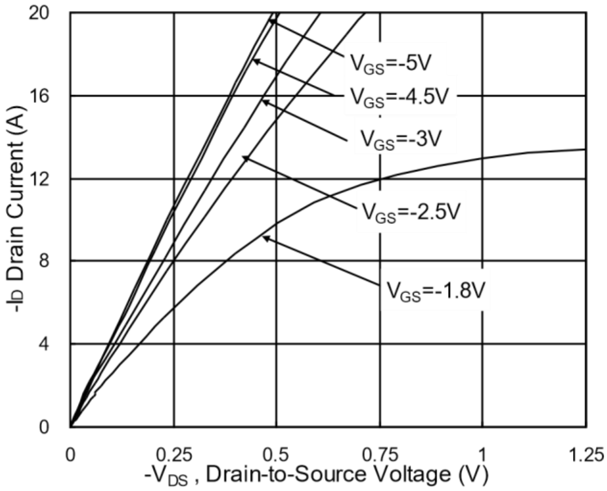


Fig.1 Typical Output Characteristics

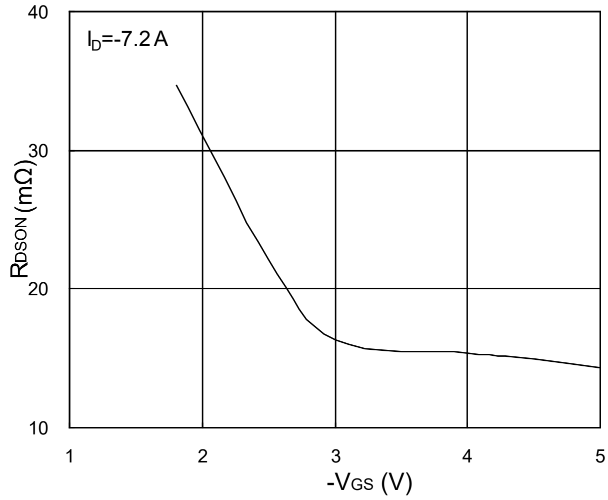


Fig.2 On-Resistance vs. Gate-Source

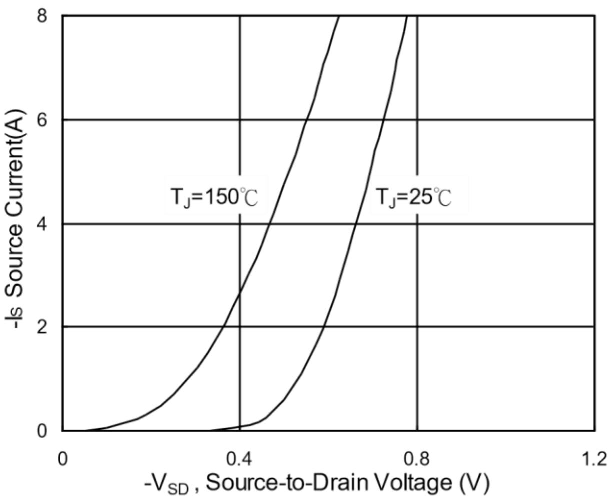


Fig.3 Forward Characteristics Of Reverse

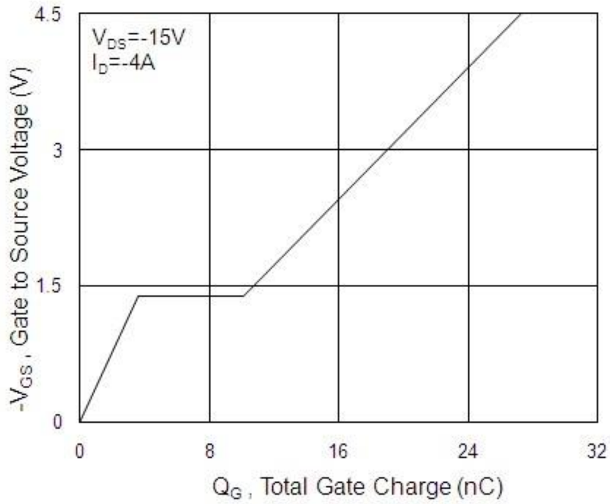


Fig.4 Gate-Charge Characteristics

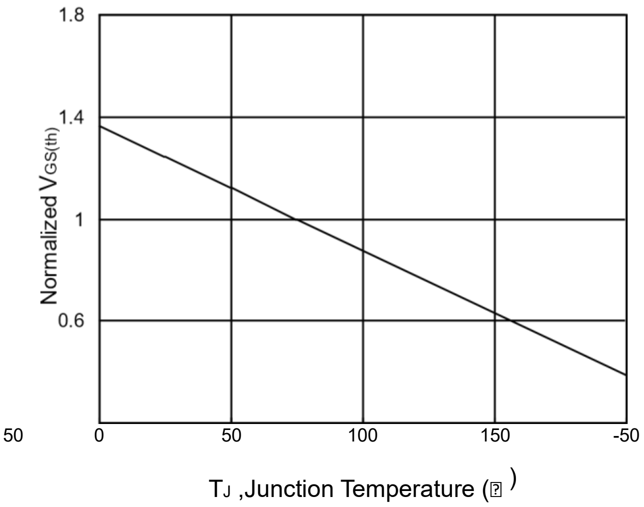


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

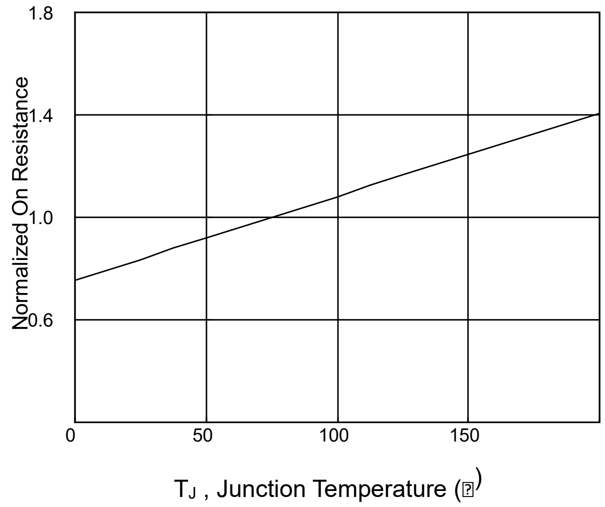


Fig.6 Normalized R_{DSON} vs. T_J

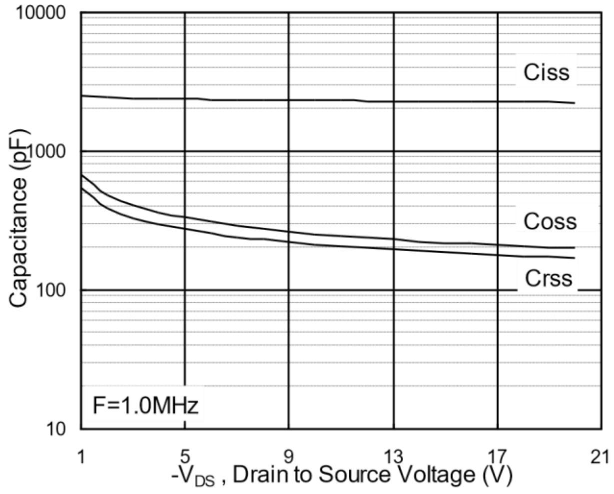


Fig.7 Capacitance

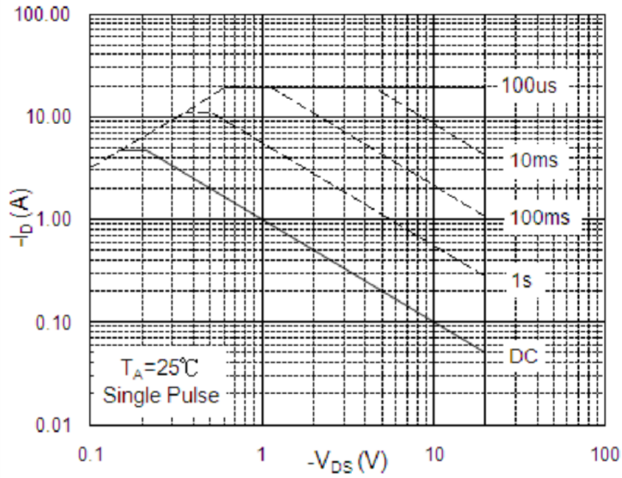


Fig.8 Safe Operating Area

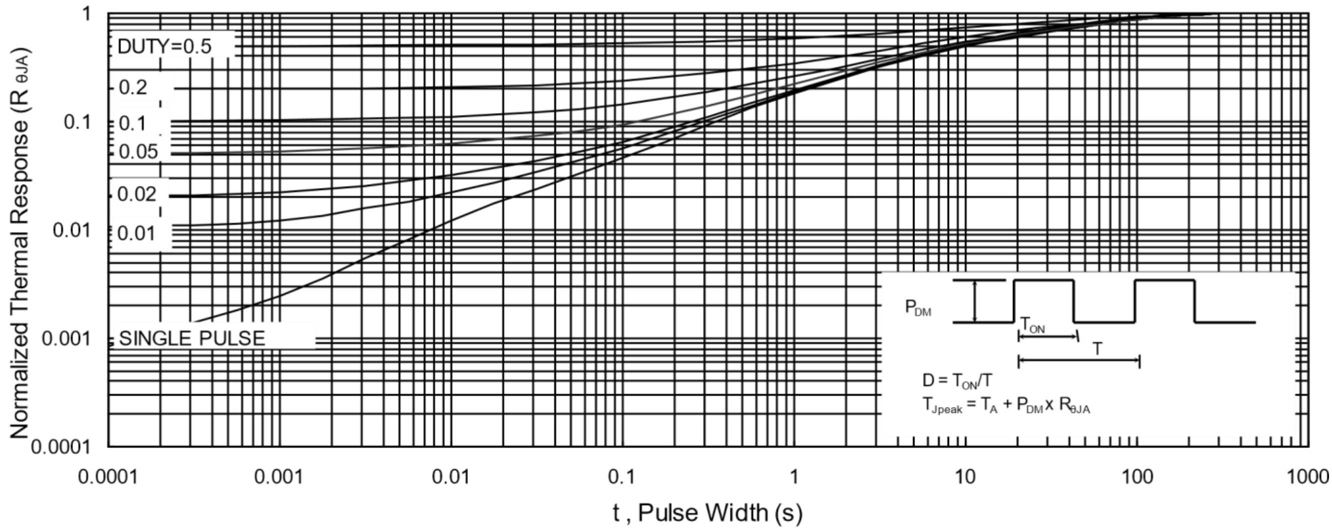
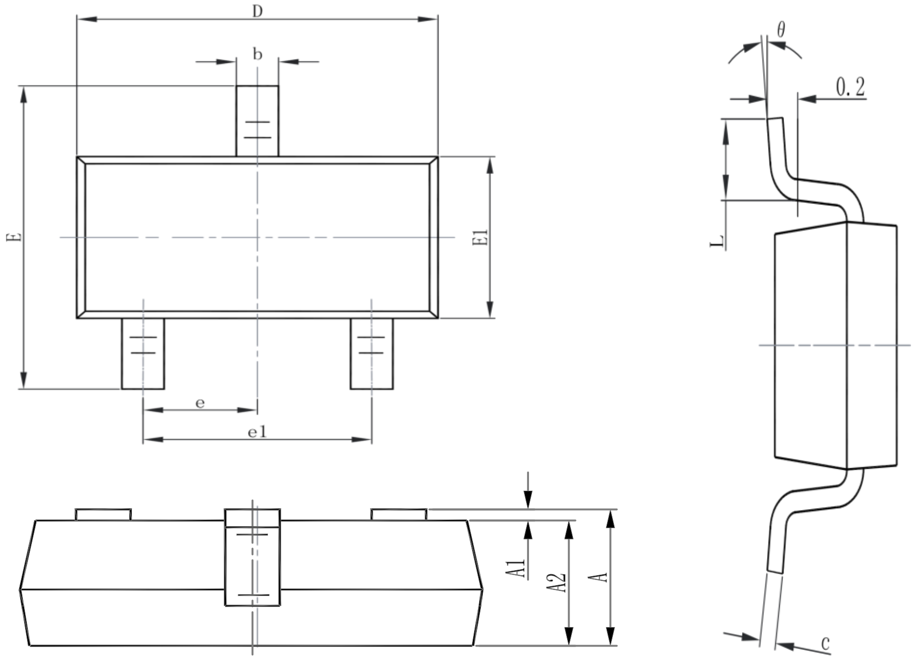


Fig.9 Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-SOT23-3



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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