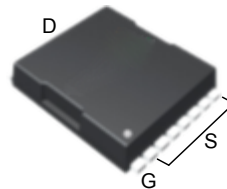


Features

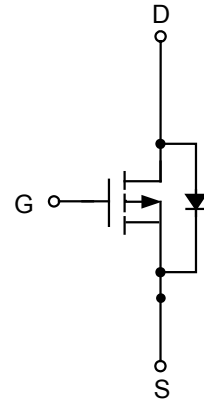
- 60V/-180A
 $R_{DS(ON)}=5m\Omega(\text{typ.})@V_{GS}=-10V$
 $R_{DS(ON)}=6m\Omega(\text{typ.})@V_{GS}=-4.5V$
- 100% UIS + R_g Tested
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)



Pin Description



TO-LL



P-Channel MOSFET

Applications

- SMPS Synchronous Rectification
- Load Switch
- DC-DC Conversion
- Or-ing

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
XPX180P06LL	XPX180P06LL	TOLL	-	-	2000

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Rating	Unit
Common Ratings			
V_{DSS}	Drain-Source Voltage	-60	V
V_{GSS}	Gate-Source Voltage	± 20	
T_J	Maximum Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	
I_S	Diode Continuous Forward Current	$T_C=25^\circ\text{C}$ -180	A
I_D	Continuous Drain Current	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$ -180 -100	
I_{DM}^a	Pulsed Drain Current	$T_C=25^\circ\text{C}$ -400	W
P_D	Maximum Power Dissipation	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$ 395 205	
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State 0.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	Steady State 50	$^\circ\text{C}/\text{W}$
I_{AS}^b	Avalanche Current, Single pulse	L=0.5mH -55	A
E_{AS}^b	Avalanche Energy, Single pulse	L=0.5mH 756	mJ

Note a : Pulse width limited by max. junction temperature.

Note b : UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature $T_J=25^\circ\text{C}$).

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

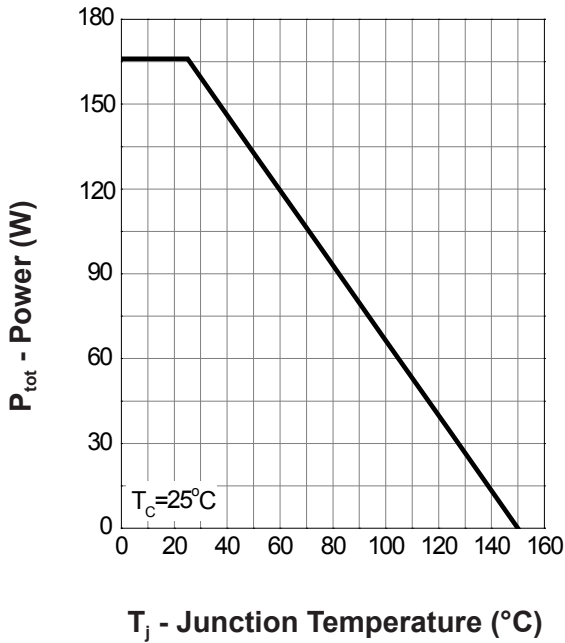
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=-250\mu A$	-60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-48V, V_{GS}=0V$ $T_J=85^\circ\text{C}$	-	-	-1	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=-250\mu A$	-1.0	-1.7	-2.5	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
$R_{DS(on)}^c$	Drain-Source On-state Resistance	$V_{GS}=-10V, I_{DS}=-30A$ $V_{GS}=-4.5V, I_{DS}=-20A$	-	5	6	m Ω
			-	6	8	m Ω
Diode Characteristics						
V_{SD}^c	Diode Forward Voltage	$I_{SD}=-1A, V_{GS}=0V$	-	-0.7	-1.1	V
t_{rr}	Reverse Recovery Time	$I_{SD}=-20A, dI_{SD}/dt=100A/\mu s$	-	29	-	ns
Q_{rr}	Reverse Recovery Charge		-	18	-	nC
Dynamic Characteristics^d						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, f=1\text{MHz}$	-	3.2	-	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$	-	2780	3614	pF
C_{oss}	Output Capacitance	$V_{DS}=-20V,$	-	426	-	
C_{riss}	Reverse Transfer Capacitance	Frequency=1.0MHz	-	331	-	
$t_{d(ON)}$	Turn-on Delay Time		-	13	24	ns
t_r	Turn-on Rise Time	$V_{DD}=-20V, R_L=20\Omega,$	-	11	20	
$t_{d(OFF)}$	Turn-off Delay Time	$I_{DS}=-1A, V_{GEN}=-10V,$	-	94	170	
t_f	Turn-off Fall Time	$R_G=6\Omega$	-	48	87	
Gate Charge Characteristics^d						
Q_g	Total Gate Charge	$V_{DS}=-20V, V_{GS}=-4.5V,$ $I_{DS}=-30A$	-	32	-	nC
Q_g	Total Gate Charge		-	63	88	
Q_{gs}	Gate-Source Charge	$V_{DS}=-20V, V_{GS}=-10V,$ $I_{DS}=-30A$	-	10.2	-	
Q_{gd}	Gate-Drain Charge		-	17.3	-	

Note c : Pulse test ; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

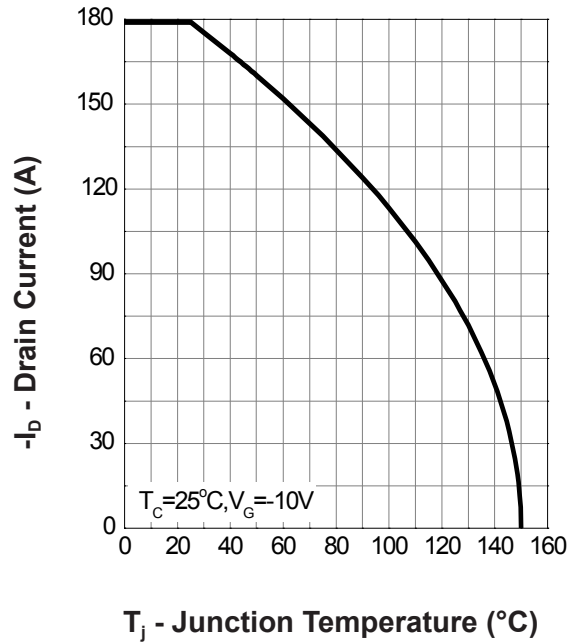
Note d : Guaranteed by design, not subject to production testing.

Typical Operating Characteristics

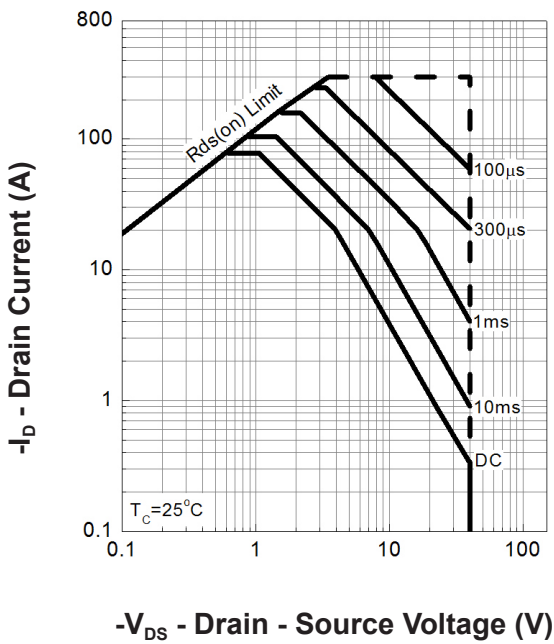
Power Dissipation



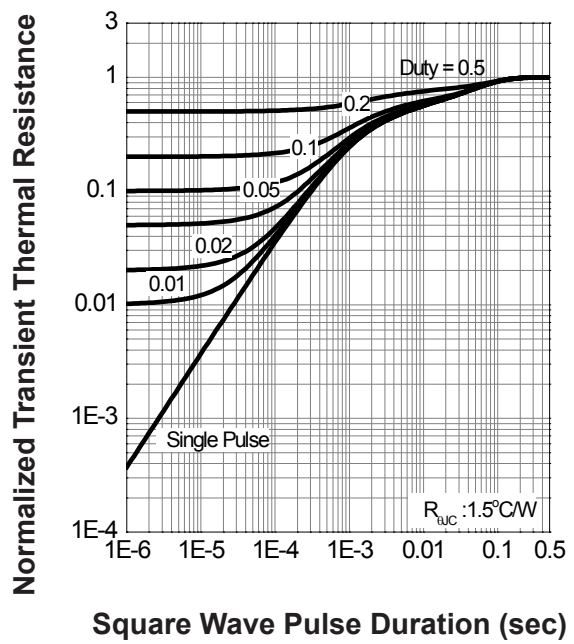
Drain Current



Safe Operation Area

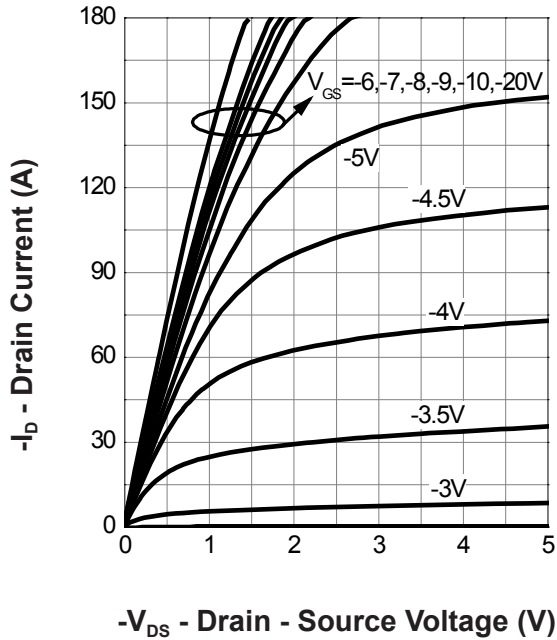


Thermal Transient Impedance

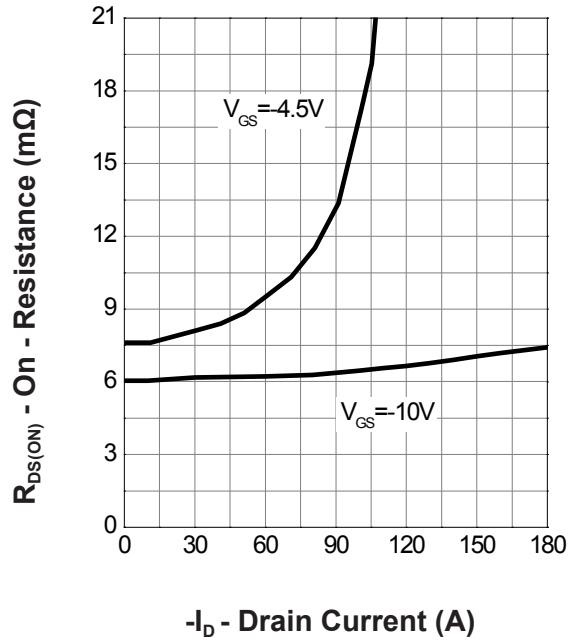


Typical Operating Characteristics(Cont.)

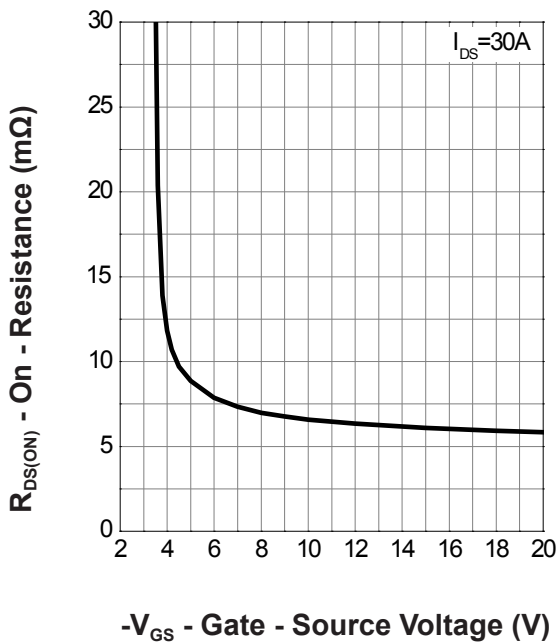
Output Characteristics



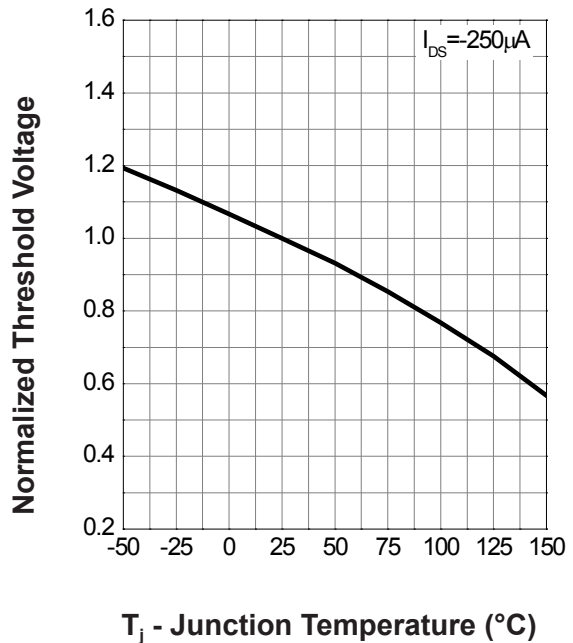
Drain-Source On Resistance



Gate-Source On Resistance

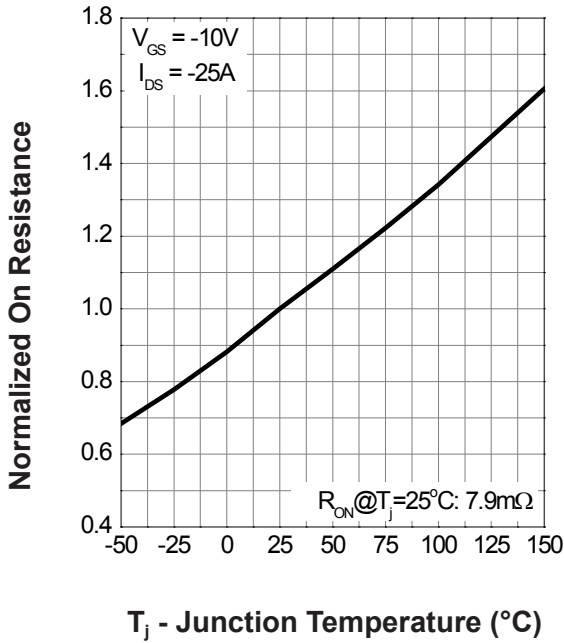


Gate Threshold Voltage

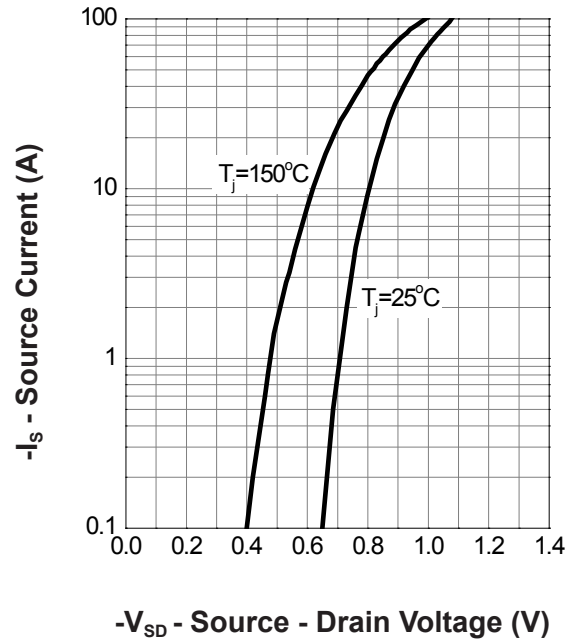


Typical Operating Characteristics(Cont.)

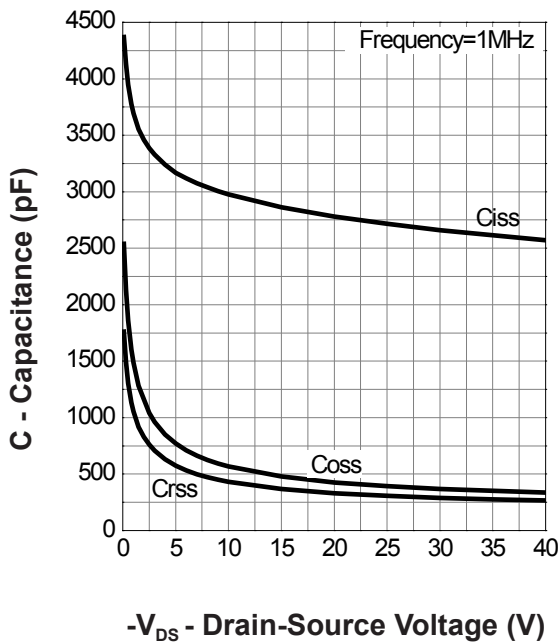
Drain-Source On Resistance



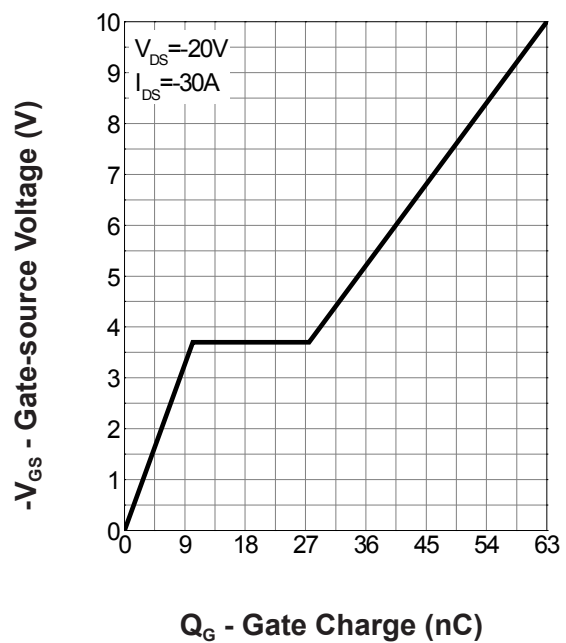
Source-Drain Diode Forward



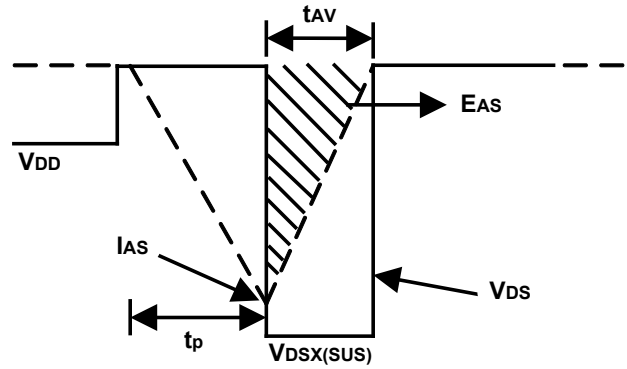
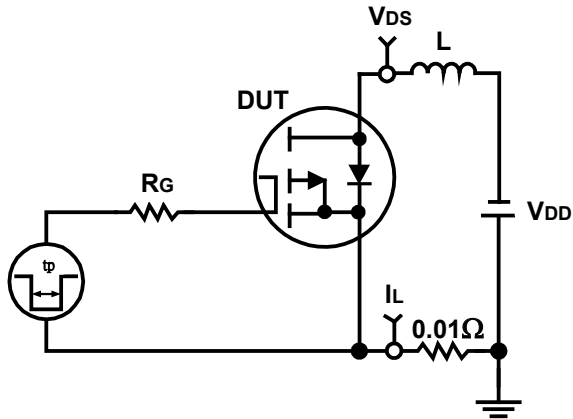
Capacitance



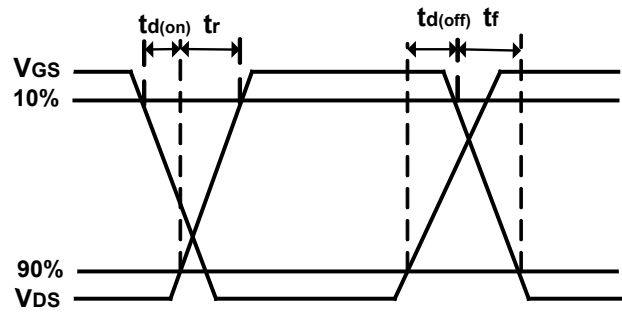
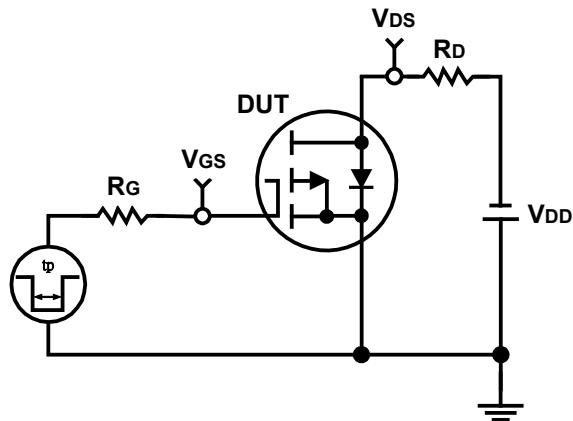
Gate Charge



Avalanche Test Circuit and Waveforms

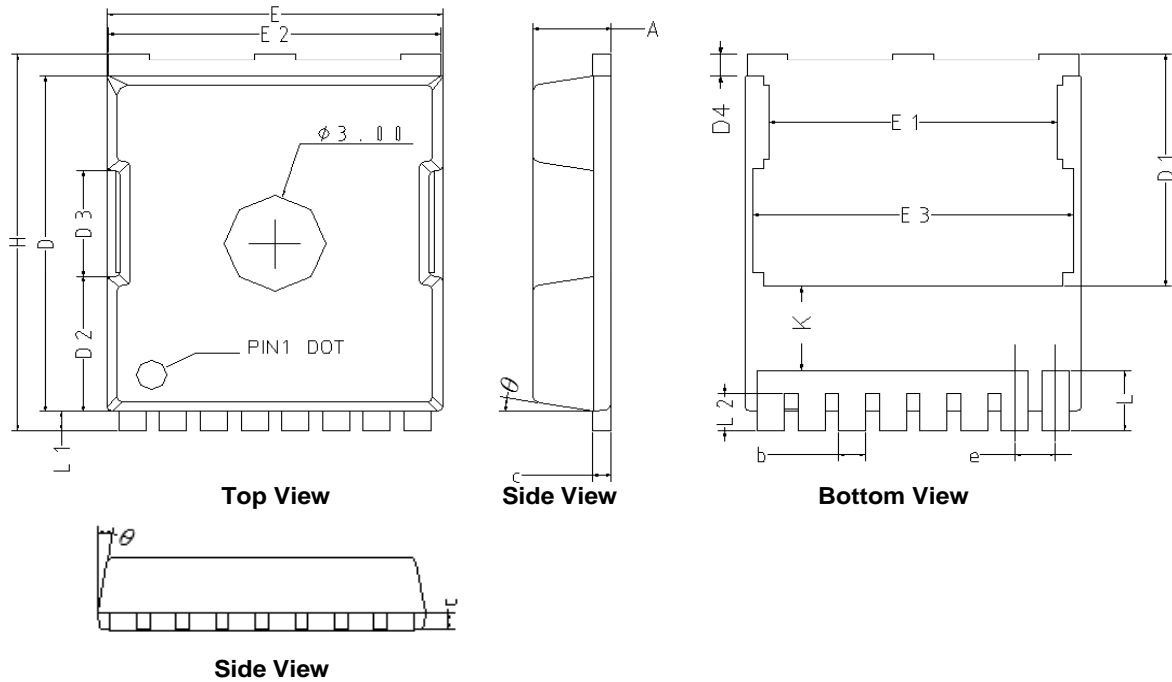


Switching Time Test Circuit and Waveforms



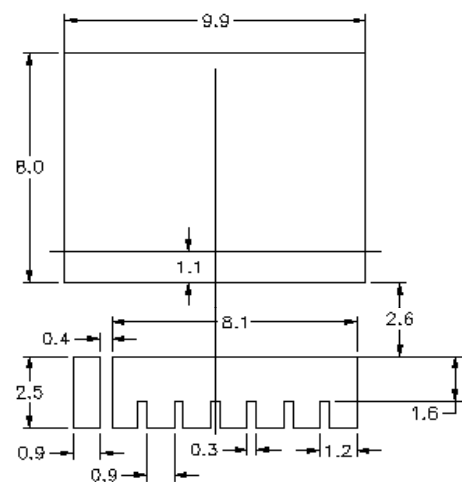
Package Information

TOLL



SYMBOLS	TO-LL			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.20	2.40	0.087	0.094
b	0.70	0.90	0.028	0.035
c	0.40	0.60	0.016	0.024
D	10.23	10.63	0.403	0.419
D1	7.05	7.45	0.278	0.293
D2	3.98	4.38	0.157	0.172
D3	3.10	3.50	0.122	0.138
D4	0.50	0.90	0.020	0.035
E	9.70	10.10	0.382	0.398
E1	8.30	8.70	0.327	0.343
E2	9.60	10.00	0.378	0.394
E3	9.26	9.66	0.365	0.380
H	11.53	11.93	0.454	0.470
e	1.2 BSC		0.0472 BSC	
K	2.43	2.83	0.096	0.111
L	1.65	2.05	0.065	0.081
L1	0.40	0.80	0.016	0.031
L2	0.95	1.35	0.037	0.053
θ	6°	10°	6°	10°

RECOMMENDED LAND PATTERN



UNIT: mm

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245°C ±5°C	5sec ±1 sec
Pb-Free device	260°C +0/-5°C	5sec ±1 sec



This integrated circuit can be damaged by ESD. UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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