XPX0113TU

100V N-Channel Enhancement Mode Power MOSFET

RoHS COMPLIANT

● Features

V_{DS} = 100V,

I_D = 190A（at V_{GS} = 10V）

$R_{DS(ON)}$ @V_{GS}= 10V,< 4.7mΩ　< 4.4mΩ *

$R_{DS(ON)}$ @V_{GS}= 6V, < 6 mΩ　< 5.5mΩ *

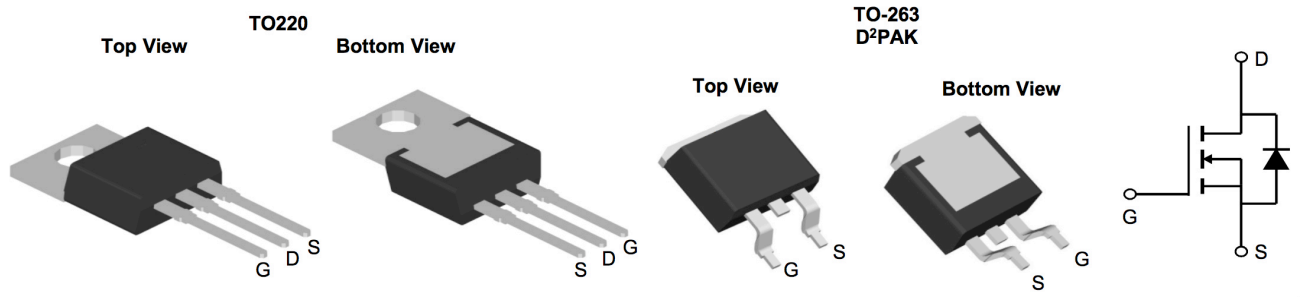
100% UIS Tested

100% Rg Tested

● General Description

- Trench Power TBO technology
- Low RDS(ON)
- Low Gate Charger
- Optimized fast-switching applications
- BMS battery protection
- Synchronous Rectifiers in DC/DC and AC/DC Converters
- Industrial and Motor Drive applications

● Pin Configurations



● Absolute Maximum Ratings @T_A=25℃ unless otherwise noted

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current G	T_C=25°C	I_D	190	A
	T_C=100°C		120	
Pulsed Drain Current C		I_{DM}	425	A
Continuous Drain Current	T_A=25°C	I_{DSM}	29	A
	T_A=70°C		23	
Avalanche Current C		I_{AS}	77	A
Avalanche energy L=0.1mH C		EAS	296	mJ
V_{DS} Spike	10μs	V_{SPIKE}	120	V

Power Dissipation B	T_C=25°C	P_D	326	W
	T_C=100°C		163	
Power Dissipation A	T_C=25°C	P_{DSM}	8.3	W
	T_C=70°C		5.3	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 to 175	°C

- **Thermal Resistance Ratings**

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient A	t ≤ 10 s	$R_{\theta JA}$	12	15	°C/W
Maximum Junction-to-Ambient A, D	Steady State		50	60	
Maximum Junction-to-Case	Steady State	$R_{\theta JC}$	0.36	0.46	

Surface mount package TO263

- **Electrical Characteristics** @T_A=25℃ unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D= 250μA	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0V	--	--	1	μA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_{DS}= 250μA	2.3	2.8	3.4	V
Gate Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	--	--	±100	nA
Drain-Source On-state Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A TO220	--	3.9	4.7	mΩ
		V_{GS} = 6V, I_D = 20A TO220	--	4.7	6	
		V_{GS} = 10V, I_D = 20A TO263	--	3.6	4.4	
		V_{GS} = 6V, I_D = 20A TO263	--	4.1	5.5	
Forward Transconductance	g_{FS}	V_{DS}= 5V, I_D= 20A	--	90	--	S
Diode Forward Voltage	V_{SD}	I_S= 1A , V_{GS}=0V	--	0.68	1	V
Max Body-Diode Continuous CurrentG	I_S		--	--	120	A
Switching						
Total Gate Charge	Q_g(10V)	V_{DS}=50V,I_D=20A, V_{GS}=10V	--	93	135	nC
Gate-Source Charge	Q_{gs}		--	23	--	nC
Gate-Drain Charge	Q_{gd}		--	16	--	nC
Turn-on Delay Time	$t_{d(on)}$	V_{GS}=10V V_{DS}=50V ,R_L=2.5Ω R_{GEN}=3Ω	--	21	--	ns
Turn-on Rise Time	t_r		--	22	--	ns
Turn-off Delay Time	$t_{d(off)}$		--	58	--	ns
Turn-Off Fall Time	t_f		--	20	--	ns

Body Diode Reverse Recovery Time	t_{rr}	I_F=20A, di/dt=500A/μs	--	49	--	ns
Body Diode Reverse Recovery Charge	Q_{rr}	I_F=20A, di/dt=500A/μs	--	460	--	nC
Dynamic						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V, f=1.0MHz	--	7085	--	pF
Output Capacitance	C_{oss}		--	605	--	pF
Reverse Transfer Capacitance	C_{rss}		--	32	--	pF
Gate resistance	R_g	f=1.0MHz	0.4	0.8	1.2	Ω

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

- **Typical Performance Characteristics（TJ = 25 °C, unless otherwise noted）**

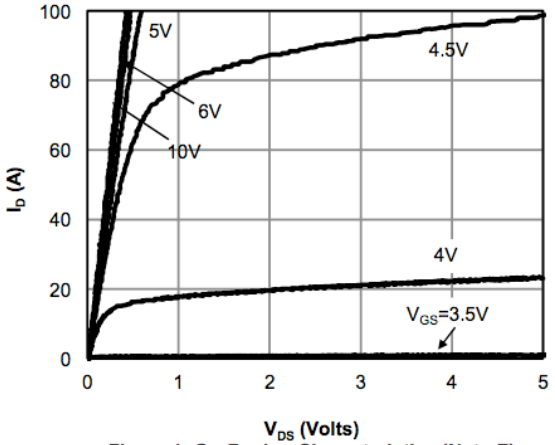


Figure 1: On-Region Characteristics (Note E)

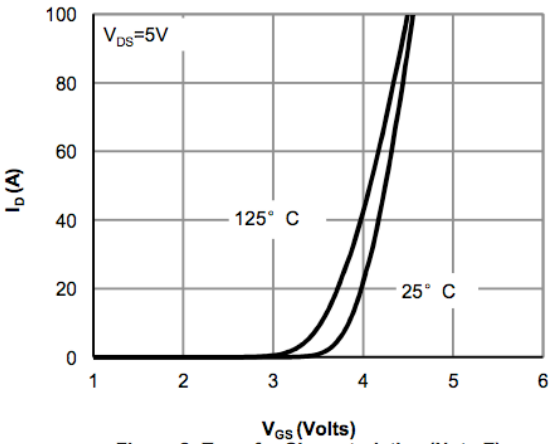


Figure 2: Transfer Characteristics (Note E)

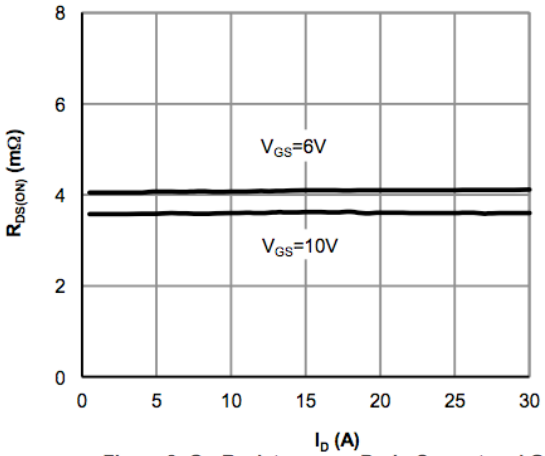


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

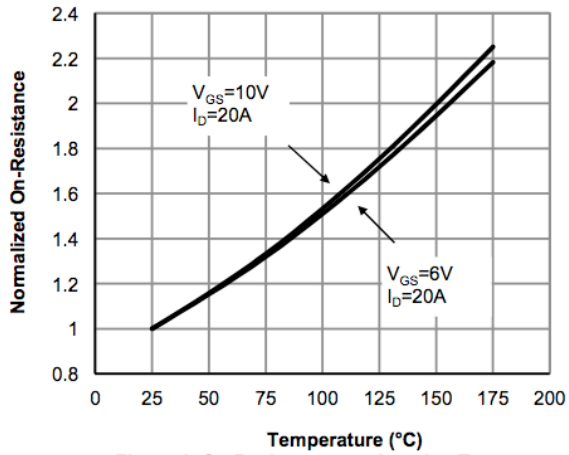


Figure 4: On-Resistance vs. Junction Temperature (Note E)

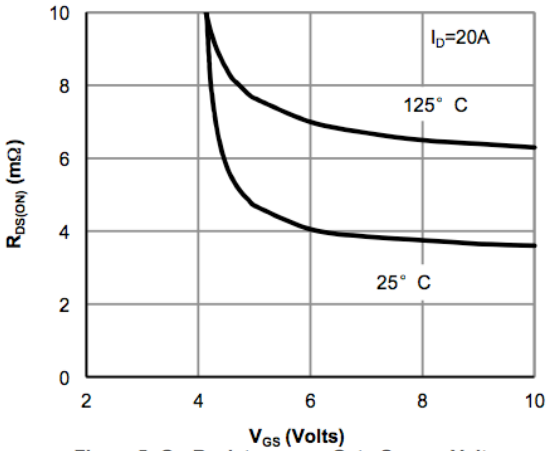


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

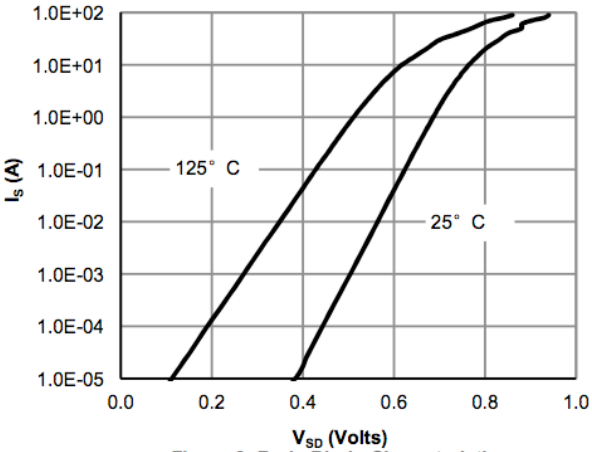


Figure 6: Body-Diode Characteristics (Note E)

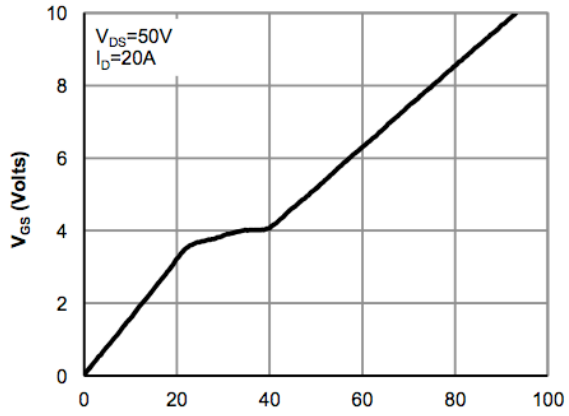


Figure 7: Gate-Charge Characteristics

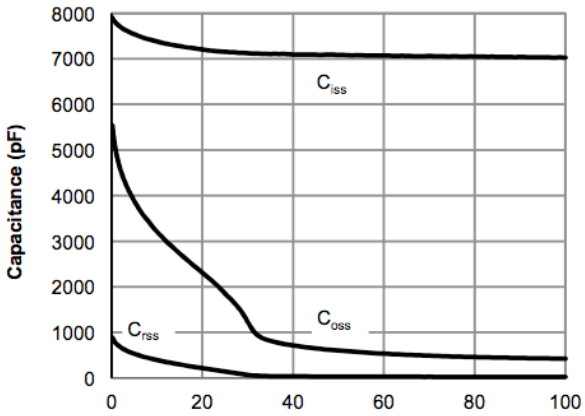


Figure 8: Capacitance Characteristics

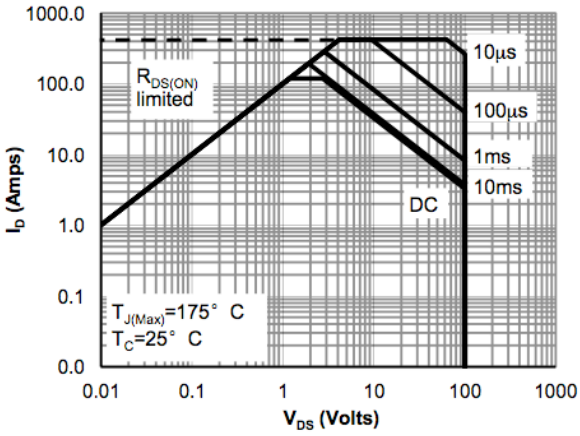


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

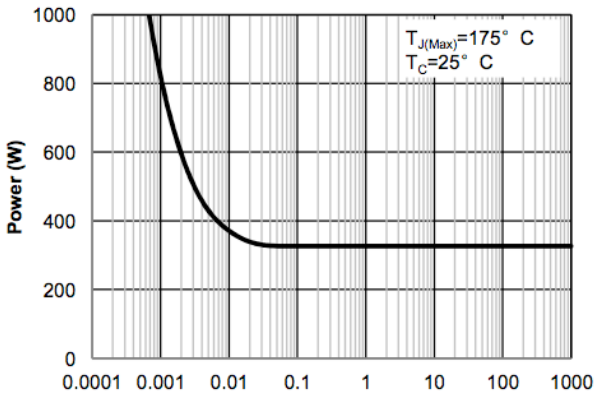


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

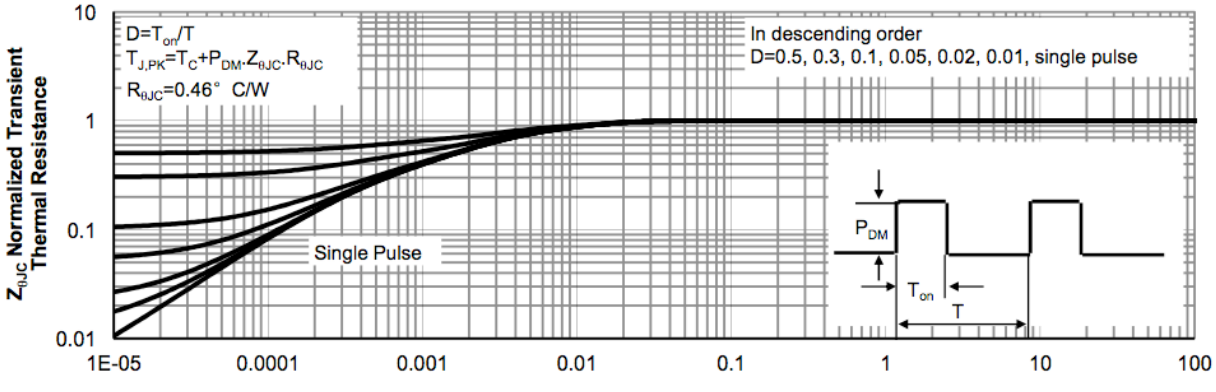


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

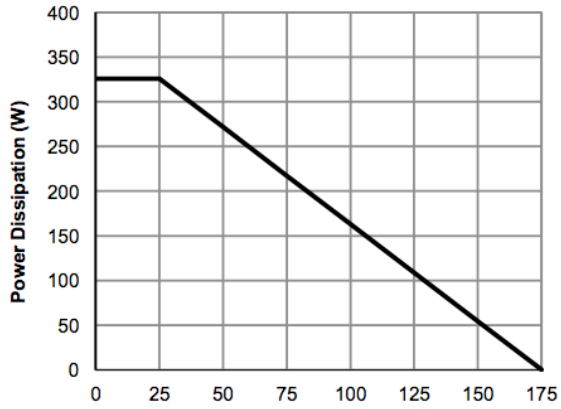


Figure 12: Power De-rating (Note F)

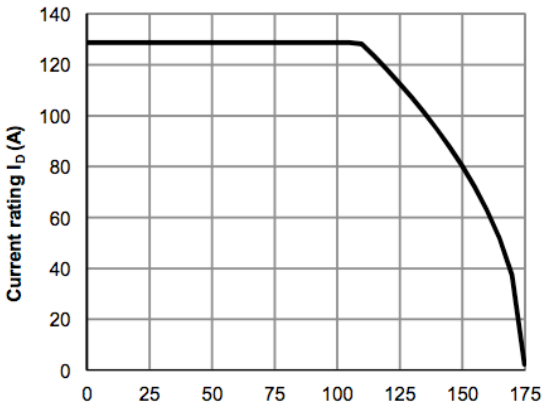


Figure 13: Current De-rating (Note F)

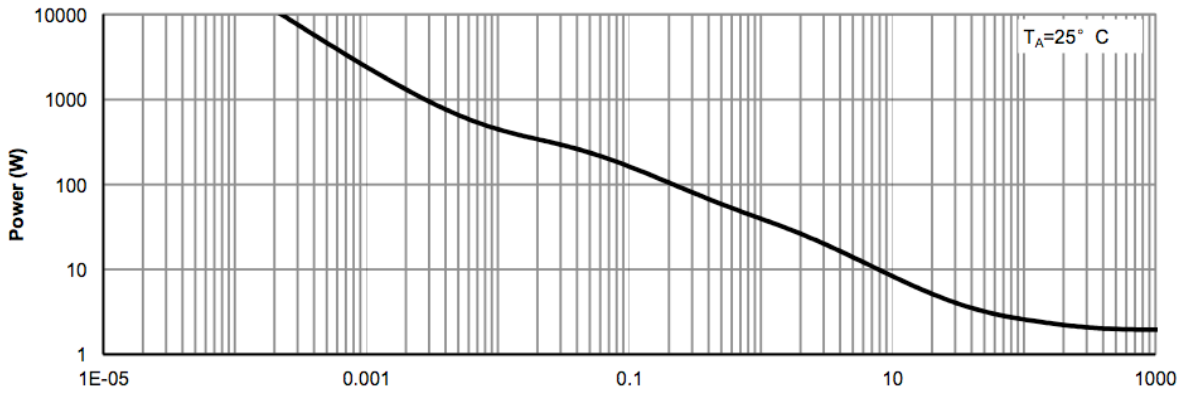


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

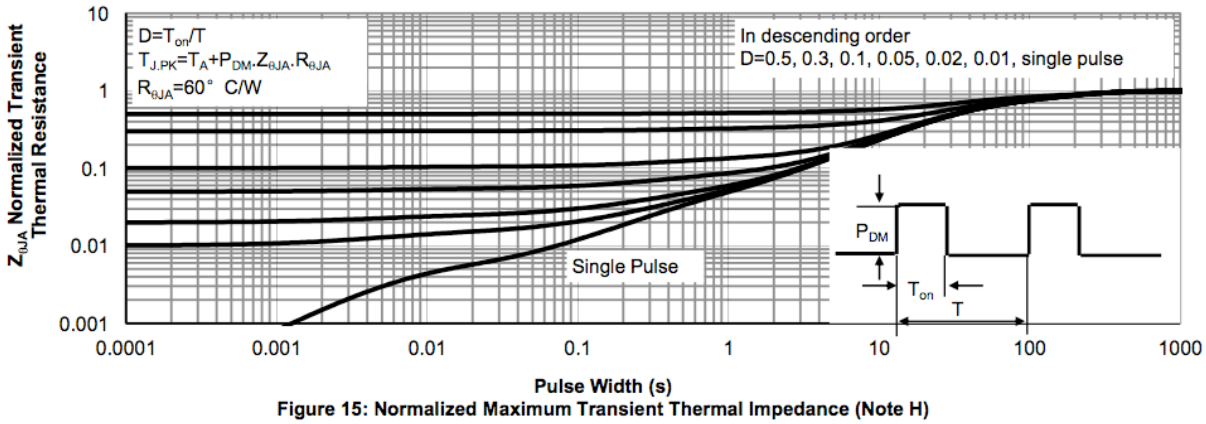


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

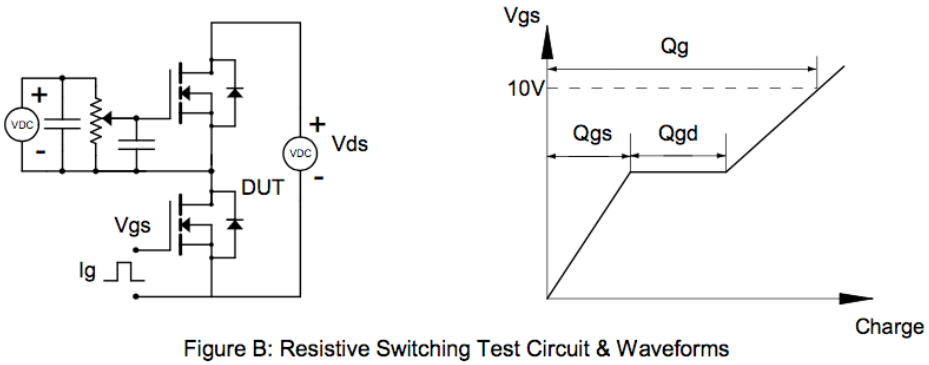


Figure B: Resistive Switching Test Circuit & Waveforms

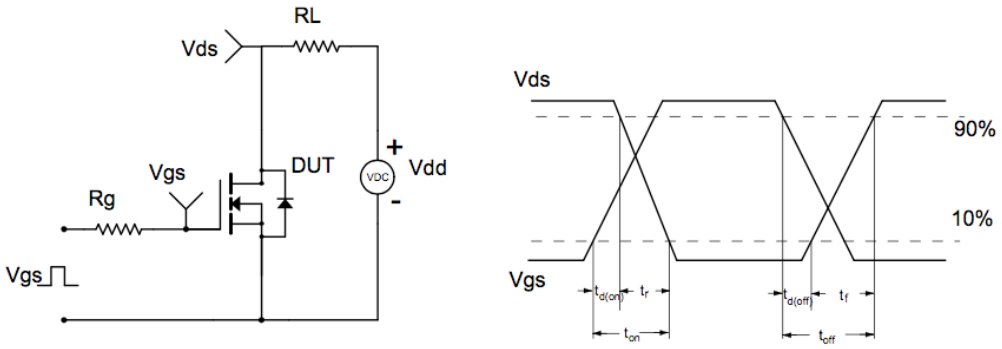


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

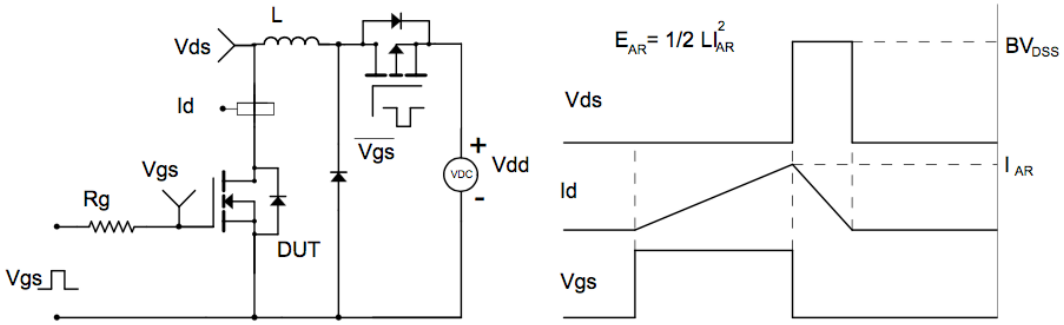
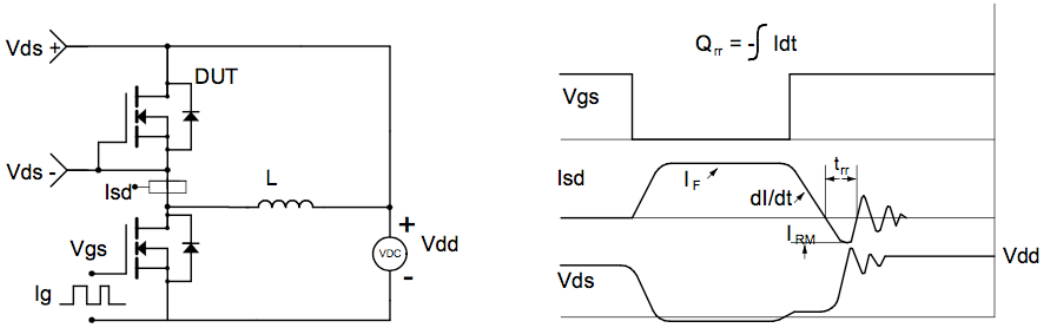
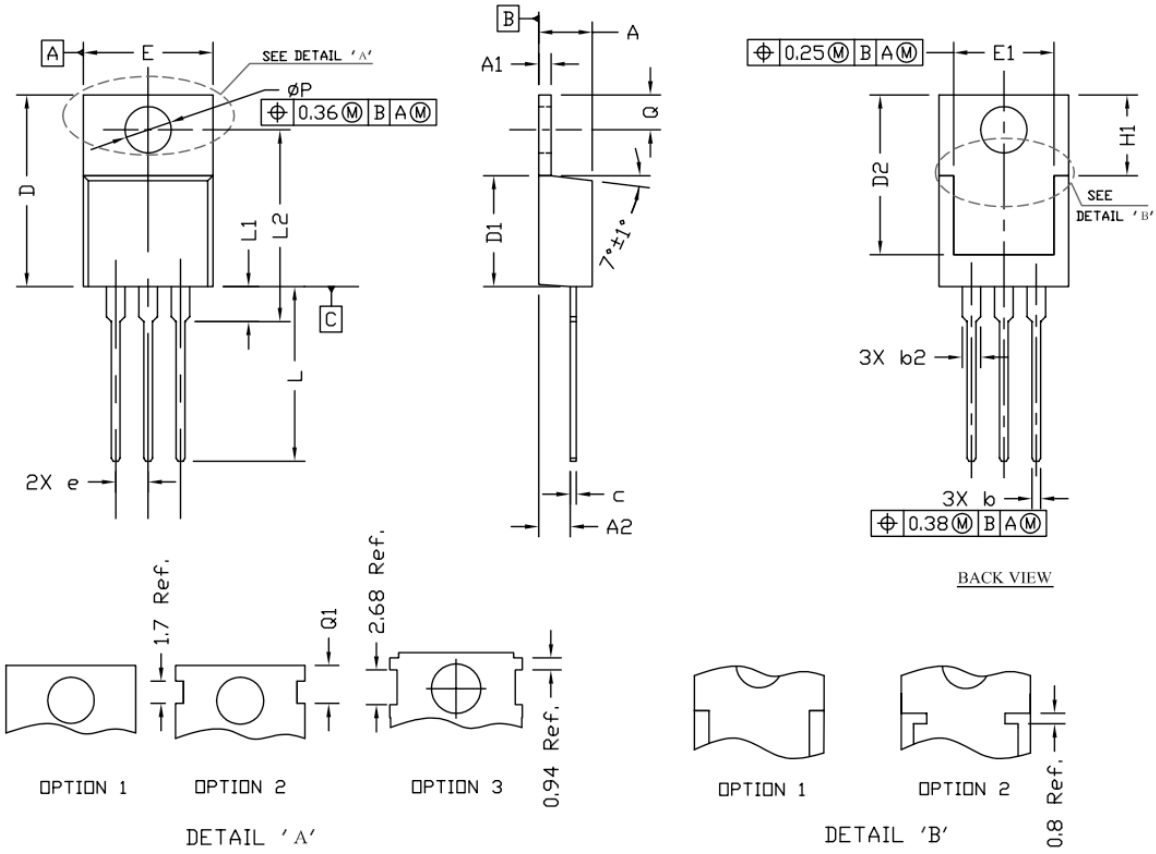


Figure D: Diode Recovery Test Circuit & Waveforms

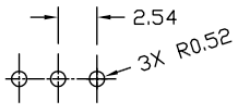


- **Package Information**

TO220 PACKAGE OUTLINE



RECOMMENDATION OF HOLE PATTERN

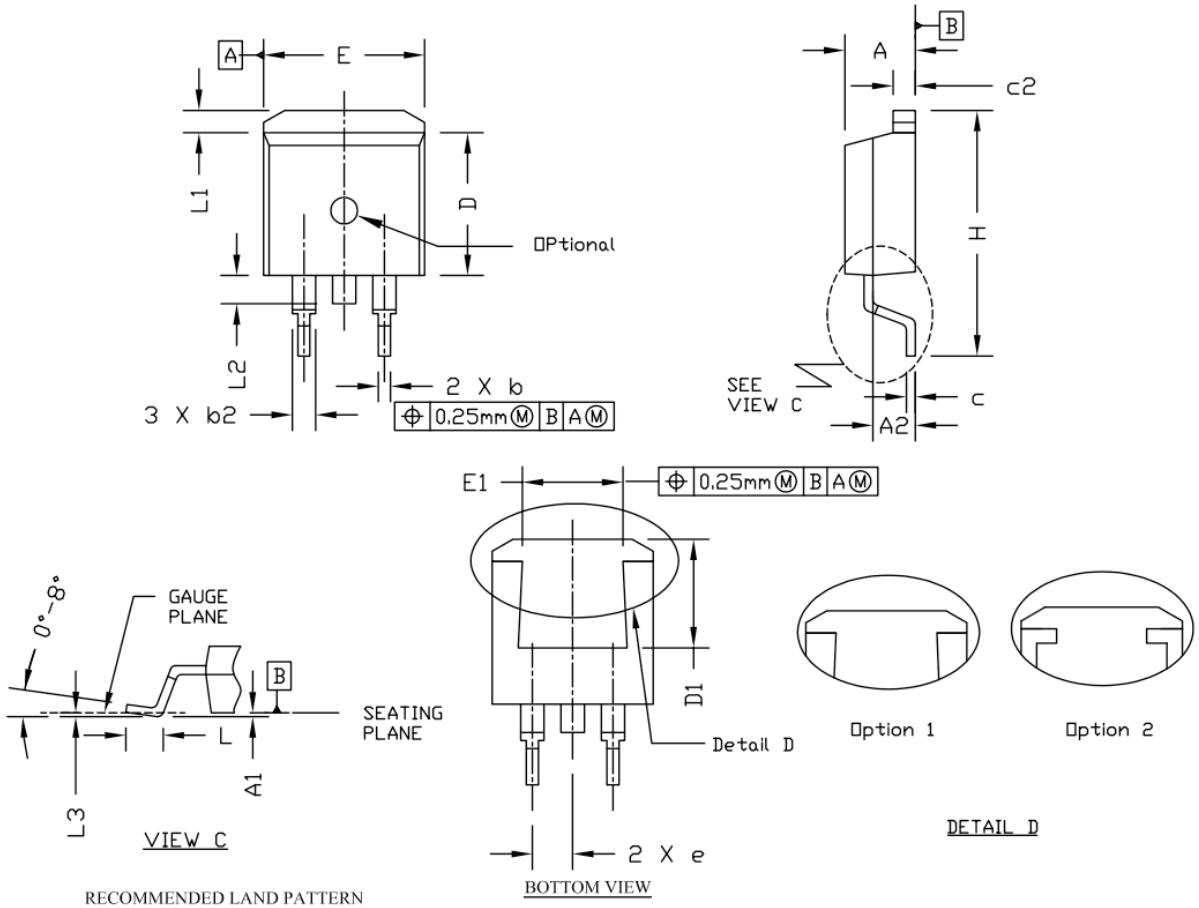


UNIT: mm

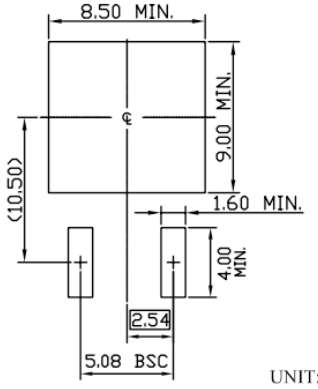
NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.30	4.45	4.72	0.169	0.175	0.186
A1	1.15	1.27	1.40	0.045	0.050	0.055
A2	2.20	2.67	2.90	0.087	0.105	0.114
b	0.69	0.81	0.95	0.027	0.032	0.037
b2	1.17	1.37	1.45	0.046	0.050	0.068
c	0.36	0.38	0.60	0.014	0.015	0.024
D	14.50	15.44	15.80	0.571	0.608	0.622
D1	8.59	9.14	9.65	0.338	0.360	0.380
D2	11.43	11.73	12.48	0.450	0.462	0.491
e	2.54 BSC			0.100 BSC.		
E	9.66	10.03	10.54	0.380	0.395	0.415
E1	6.22	---	---	0.245	---	---
H1	6.10	6.30	6.50	0.240	0.248	0.256
L	12.27	12.82	14.27	0.483	0.505	0.562
L1	2.47	---	3.90	0.097	---	0.154
L2	---	---	16.70	---	---	0.657
Q	2.59	2.74	2.89	0.102	0.108	0.114
øP	3.50	3.84	3.89	0.138	0.151	0.153
Q1	2.70	---	2.90	0.106	---	0.114

TO263(D2PAK) PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.064	4.45	4.826	0.160	0.175	0.190
A1	0.00	---	0.254	0.000	---	0.010
A2	2.20	2.67	2.90	0.087	0.105	0.114
b	0.508	0.81	0.991	0.020	0.032	0.039
b2	1.143	1.27	1.778	0.045	0.050	0.070
c	0.381	0.50	0.737	0.015	0.020	0.029
c2	1.143	1.27	1.651	0.045	0.050	0.065
D	8.382	9.14	9.652	0.330	0.360	0.380
D1	6.858	8.00	8.37	0.270	0.315	0.330
e	2.54 BSC			0.100 BSC.		
E	9.652	10.03	10.668	0.380	0.395	0.420
E1	6.223	8.00	8.37	0.245	0.315	0.330
H	14.605	15.24	15.875	0.575	0.600	0.625
L	1.778	2.54	2.794	0.070	0.100	0.110
L1	1.02	1.27	1.676	0.040	0.050	0.066
L2	1.27	1.52	1.778	0.50	0.60	0.070
L3	0.25 BSC			0.010 BSC.		

NOTE:
1. PACKAGE BODY SIDES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH SHOULD BE LESS THAN 6 MILS.
2. TOLERANCE 0.10 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. DIMENSION L IS MEASURED IN GAUGE LINE.
4. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. REFER TO JEDEC TO-263 AB.

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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