40V N-ChannelEnhancement Mode MOSFET

RoHS COMPLIANT

Description

The XPX009N04TD uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

V_{DS} =40V,I_D =320A

$R_{DS(ON)}$=0.9mΩ (typ) @ V_{GS}=10V

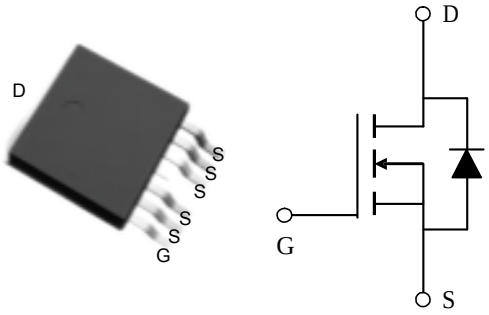
$R_{DS(ON)}$=1.3mΩ (typ) @ V_{GS}=4.5V

General Features

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- PWM
- Load Switching



Package Marking and Ordering Information

Device	Pack	Marking	Qty(PCS)
XPX009N04TD	TO-263-7	XXXXX YYYY	2000

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	320	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	226	A
Pulsed Drain Current(Note 1)	I_{DM}	1280	A
Maximum Power Dissipation	P_D	400	W
Derating factor		2.67	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	2500	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃
Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	0.38	℃/W

Electrical Characteristics (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	40		-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=160A	-	0.9	1.3	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=160A	-	100	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	11998	-	PF
Output Capacitance	C_{oss}		-	1560	-	PF
Reverse Transfer Capacitance	C_{rss}		-	1324	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=20V,R_L=15Ω, R_G=2.5Ω,V_{GS}=10V	-	42	-	nS
Turn-on Rise Time	t_r		-	41	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	150	-	nS
Turn-Off Fall Time	t_f		-	70	-	nS
Total Gate Charge	Q_g	I_D=160A,V_{DD}=20V,V_{GS}=10V	-	249	-	nC
Gate-Source Charge	Q_{gs}		-	40	-	nC
Gate-Drain Charge	Q_{gd}		-	80	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=160A	-	1.0	2.0	V
Diode Forward Current (Note 2)	I_S		-	-	320	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = 160A di/dt = 100A/μs (Note3)	-	55		nS
Reverse Recovery Charge	Qrr		-	180		nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃,V_{DD}=20V,V_G=10V,L=0.5mH,Rg=25Ω

Typical Electrical and Thermal Characteristics (Curves)

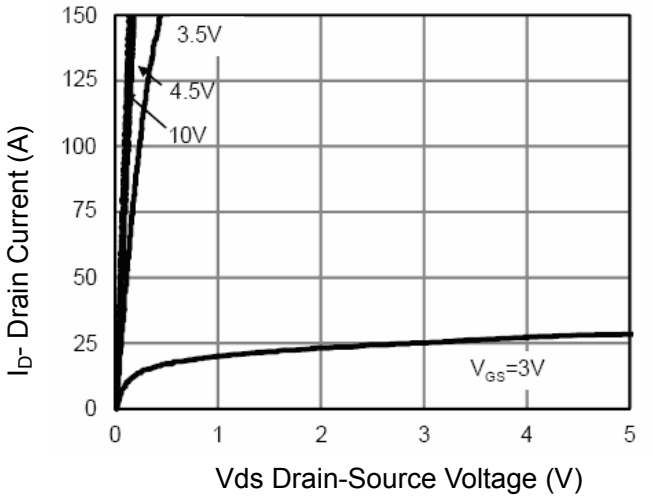


Figure 1 Output Characteristics

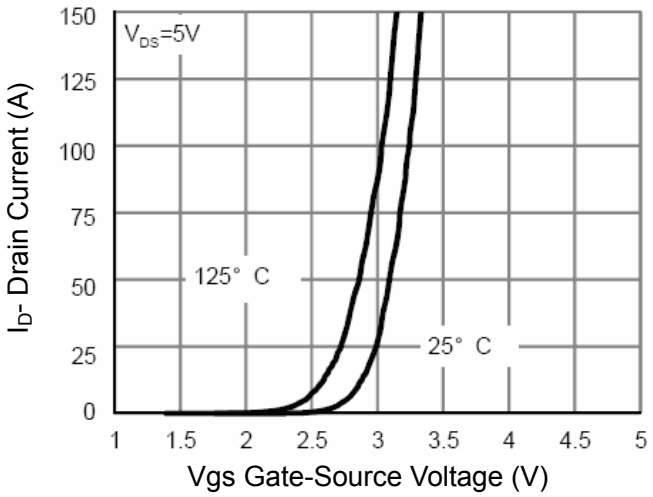


Figure 2 Transfer Characteristics

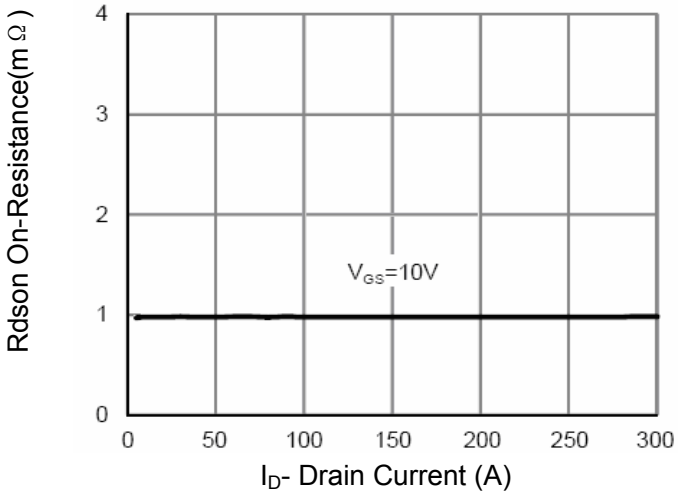


Figure 3 Rdson- Drain Current

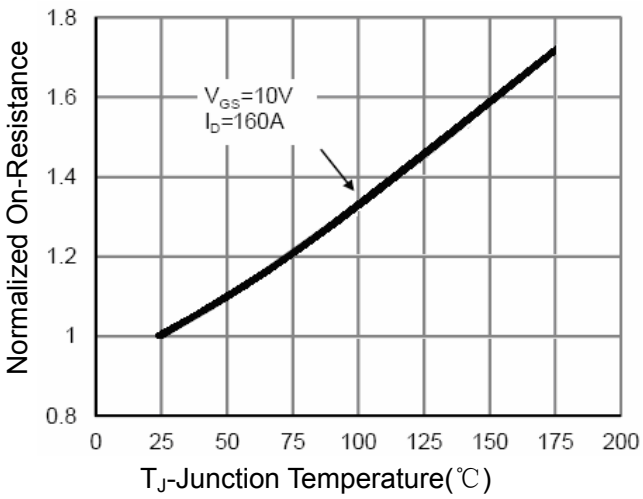


Figure 4 Rdson-JunctionTemperature

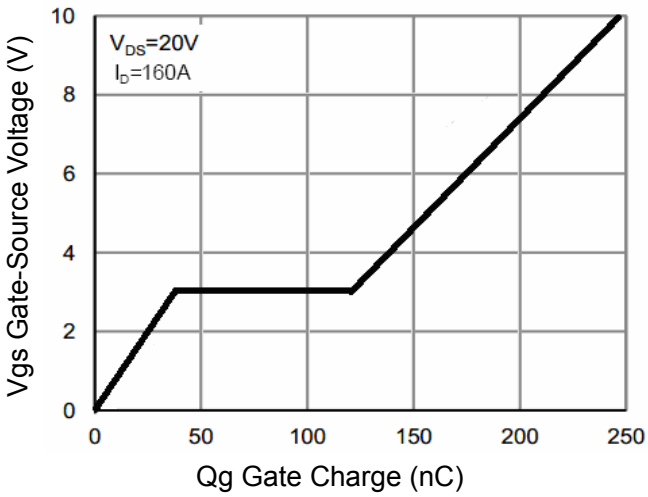


Figure 5 Gate Charge

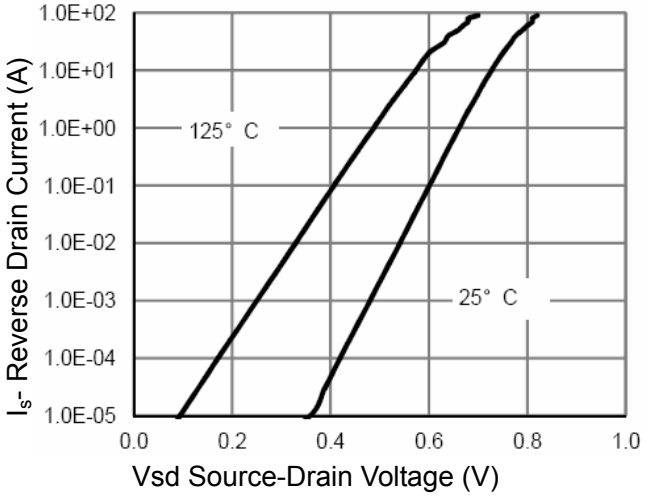


Figure 6 Source- Drain Diode Forward

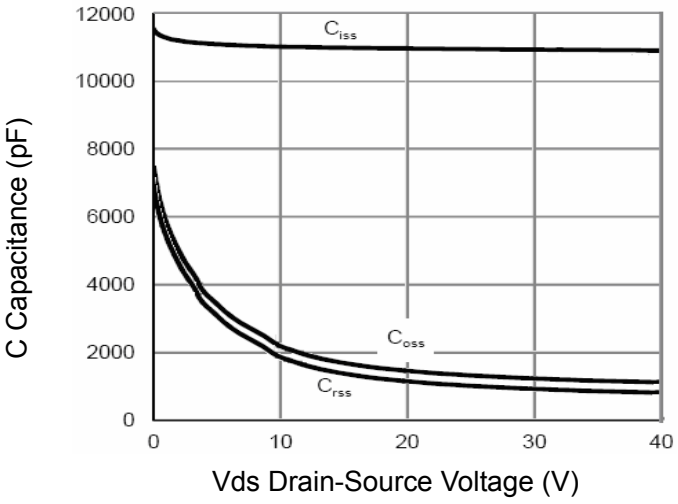


Figure 7 Capacitance vs Vds

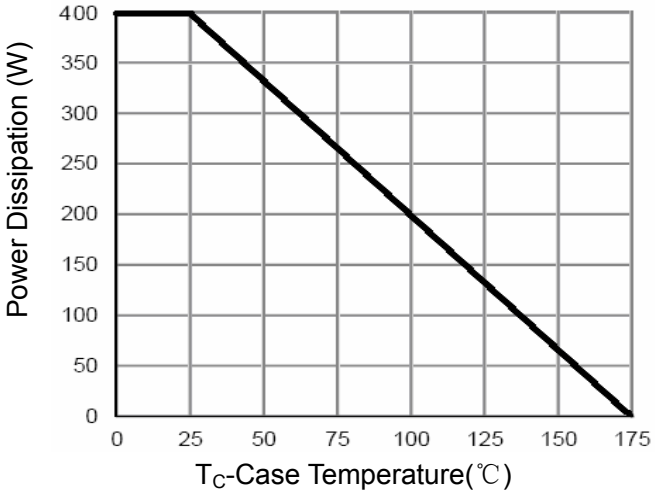


Figure 9 Power De-rating

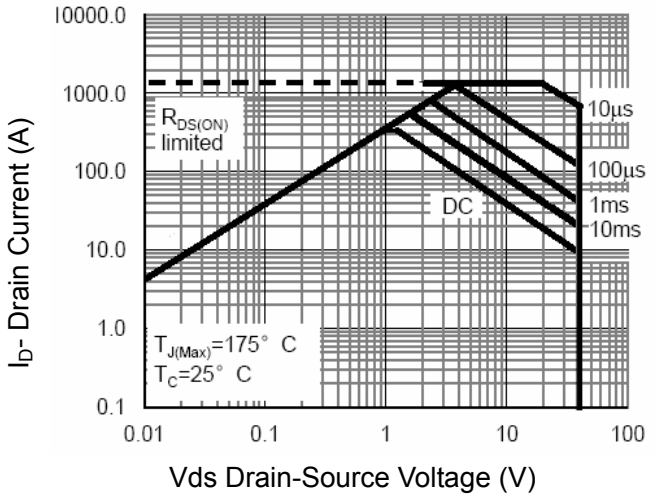


Figure 8 Safe Operation Area

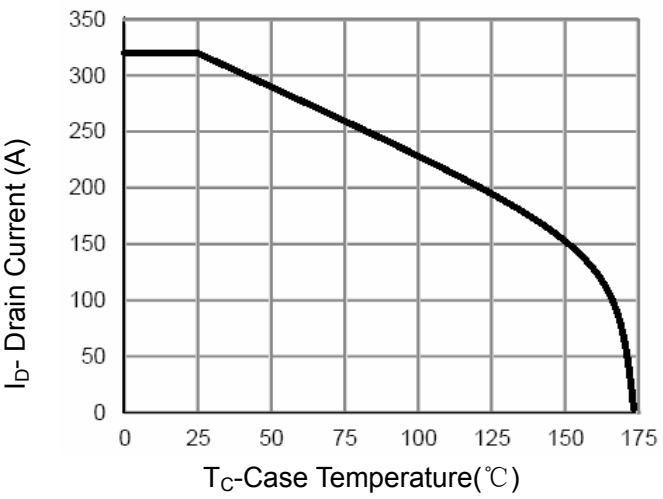


Figure 10 Current De-rating

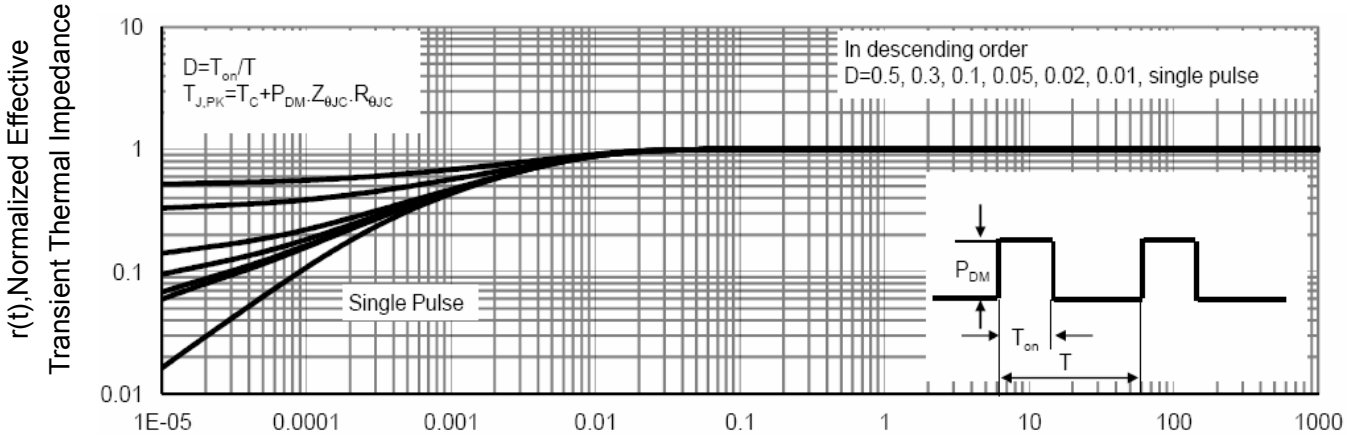
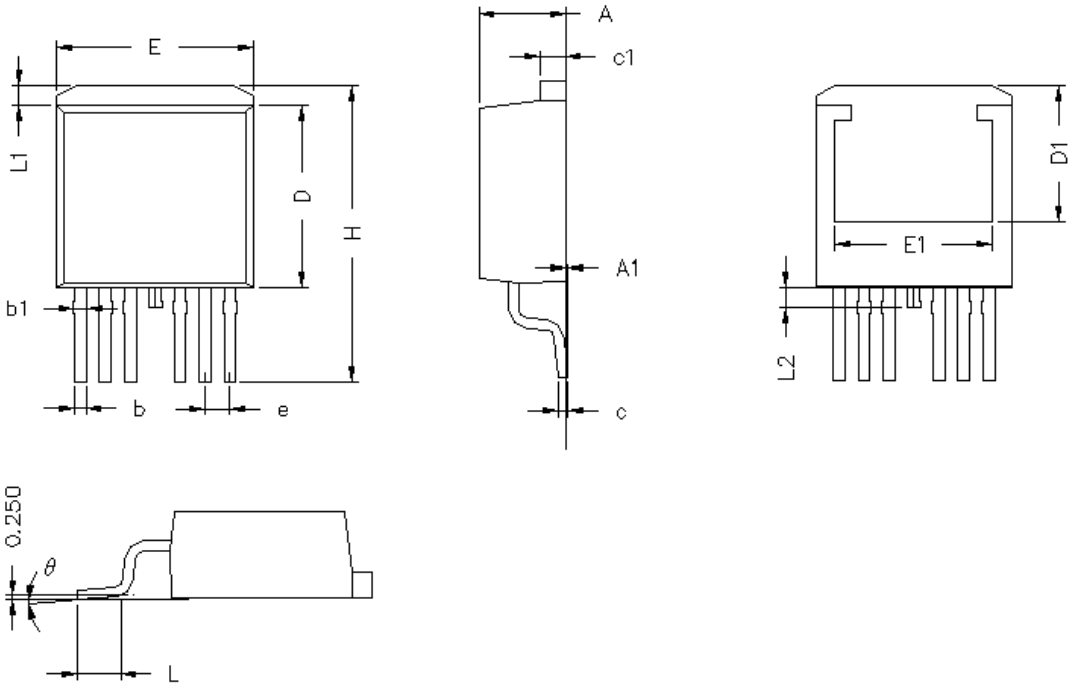


Figure 11 Normalized Maximum Transient Thermal Impedance

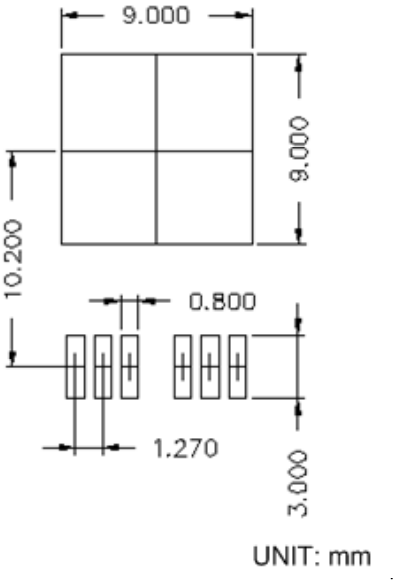
Package Information

TO-263-7



SYMBOLS	TO-263-7			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.55	0.167	0.179
A1	0.01	0.25	0.000	0.010
b	0.50	0.70	0.020	0.028
b1	0.60	0.84	0.024	0.033
c	0.40	0.60	0.016	0.024
c1	1.20	1.40	0.047	0.055
D	9.05	9.45	0.356	0.372
D1	6.90	9.00	0.272	0.354
E	9.80	10.20	0.386	0.402
E1	7.25	9.00	0.285	0.354
e	1.27 BSC		0.05 BSC	
H	14.65	15.35	0.577	0.604
L	2.40	3.00	0.094	0.118
L1	0.80	1.20	0.031	0.047
L2	0.85	1.15	0.033	0.045
θ	2°	8°	2°	8°

RECOMMENDED LAND PATTERN



UNIT: mm

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Attention:

- Any and all XPX power products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your XPX power representative nearest you before using any XPX power products described or contained herein in such applications.

- XPX power assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all XPX power products described or contained herein.

- Specifications of any and all XPX power products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

- XPX power Semiconductor CO.,LTD. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

- In the event that any or all XPX power products(including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.

- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of XPX power Semiconductor CO.,LTD.

- Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. XPX power believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

- Any and all information described or contained herein are subject to change without notice due to product/ technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the XPX power product that you intend to use.

- This catalog provides information as of Sep.2019. Specifications and information herein are subject to change without notice.